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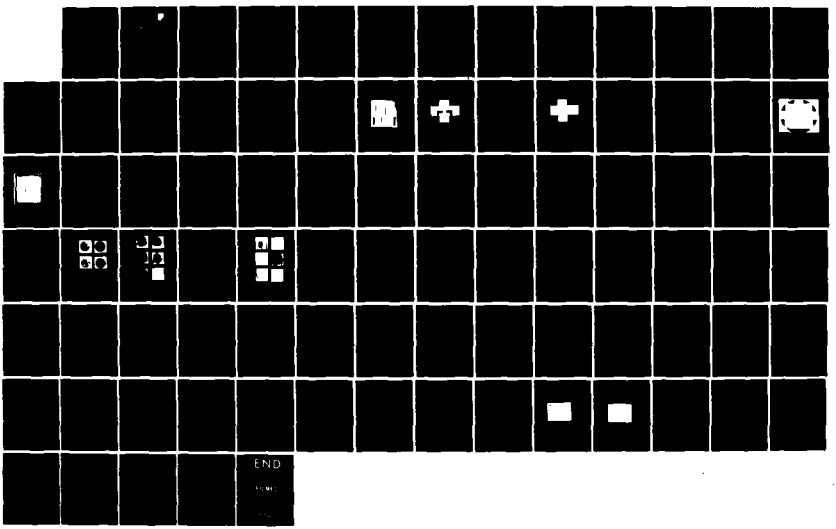

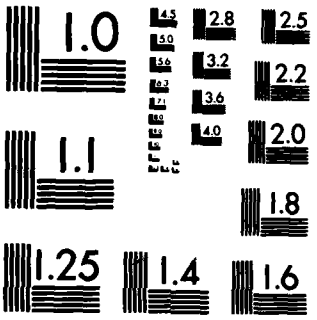

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Final Technical Report
February 1985

ANALYSIS OF TIME DEPENDENT DIELECTRIC FAILURES

Westinghouse Electric Corporation

Jin S. Kim, Paul G. McMullin and John W. Dzimianski

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ROME AIR DEVELOPMENT CENTER
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19. ABSTRACT (Continue on reverse if necessary and identify by block number)

The Time Dependent Dielectric Breakdown (TDDB) has been studied for silicon dioxide by using a staircase voltage ramping technique. The result of the ramp tests on MOS capacitors indicates a definitive substrate effect on the TDDB, which manifests itself as an enhancement of the intermediate field breakdown in the breakdown histogram. The substrate effect observed may be caused by the oxygen impurities of the starting material. This conclusion is based on the observed fact that the gate oxide grown on the high oxygen content Czochralski wafers (35 ppm) shows the breakdown enhancement, while the gate oxide grown on the low oxygen content (<1ppm) float-zone wafers does not.

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EVALUATION

Westinghouse has made a positive contribution to our understanding of time dependent dielectric failure on this contract by demonstrating the direct dependence of the breakdown voltage distribution on oxygen content in the starting wafer.

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1.0 INTRODUCTION

Dielectric breakdown of the gate oxide is one of the primary failure modes of MOS integrated circuits, particularly for VHSIC type VLSI circuits which require a very thin gate oxide due to device scaling. It is a rather complex and difficult task to assess the reliability and predict the use life of a VLSI circuit, since device failures originate from numerous and complex sources. The gate oxide failure is only one of the many device failure modes. The oxide failure mode, which is of primary interest from the device point of view, is the time dependent dielectric breakdown (TDDB). The TDDB occurs at a field lower than the intrinsic dielectric breakdown strength of the gate oxide.

The dielectric failure (TDDB) of the gate oxide has been studied intensively for the last several years. The main efforts have been directed toward better understanding the basic physics of oxide breakdown, prediction of oxide use life in MOS devices, and effective screening methods to eliminate defective parts.

A thorough understanding of the TDDB has not yet been achieved to date even though several mechanisms, such as charge injection, mechanical stress at the interface, metallic impurity diffusion/segregation at the interface, have been proposed by many investigators. Of these mechanisms, the charge injection and metallic impurity redistribution are well accepted ones at the present.

The most common method of predicting the use life of the gate oxide in MOS devices is the accelerated test. A large body of data in this area exists in the open literature. The main idea behind this technique is that the acceleration factors (primarily the temperature acceleration factor and the electric field acceleration factor) are determined from experiments and the use life is extrapolated from an accelerated life test result using the previously determined acceleration factors. In order for this acceleration test method to be valid, a correct mechanism for the failure process must be available. Otherwise, the extrapolation will be meaningless. Even though

this method is the most widely used in predicting the device life, there are some drawbacks. For example, the accelerated test often requires a temperature or electric field appreciably higher than that of the use condition or device rating, a large number of test samples, and most importantly the correct physical failure mechanism for the process. Special caution should be exercised in the accelerated test, particularly if the test is for the purpose of screening out defective parts by applying high temperature or high electric field. The effect of the high temperature and high electric field on the use life of the remaining (test-passed) devices has to be fully considered.

Another useful method of predicting use life and screening is the ramping test. For TDDB this ramping method has been claimed by Berman[1] to be superior to the accelerated life test because the assumption of the log-normal distribution of failure in time is not required. He has shown that the electric field variable in the ramp test is on the same footing as the time variable and one can be transformed to the other. He has also proposed a screening method using a proper electric field-time stress test.

During the period of the contract for the study program "Analysis of Time Dependent Dielectric Failures", the effort was focused on the following areas:

1) Survey of literatures on the time dependent dielectric breakdown of silicon dioxide in MOS devices.

2) Design of an MOS test structure (mask making) and fabrication of MOS devices using this test structure (lot processing).

3) Evaluation of oxygen and carbon content of test wafers and mechanical stress in oxide gate dielectric.

4) Electrical tests on the fabricated MOS devices.

5) Recommend and model a viable method of screening and test to predict the reliability of the gate oxide in circuits.

The objectives of this program were to study the fundamental mechanisms leading to time dependent dielectric failure in integrated circuit devices, particularly MOS structures, to devise a practical test method for predicting the mean life at normal operation of MOS devices and to provide a viable procedure for effectively screening out the unreliable parts due to defective gate oxides. A test method suggested should involve a practical test time period, a simple test structure which is representative of the MOS devices of ICs, a simple test procedure with unequivocal test result, and a minimum sample size. There are many more conditions that could be added to this list.

Life test methods depend on the mechanism associated with particular failure modes. For MOS devices, there are many failure modes associated with various physical mechanisms. For example, the failure of interconnection metal lines in an integrated circuit involves shorting or open circuiting processes which are associated with electromigration and mechanical stress effect caused by passivation layers. As indicated above, the primary concern in this program was dielectric failure of gate oxide in MOS integrated circuits. This mode of failure has been known for some time to be time-dependent (TDDB). The correct mechanism of TDDB has not been well understood. However, it is certain that the state of the gate oxide or its interface changes electrically, chemically, or mechanically with time. The TDDB phenomenon may be a complex one involving both the bulk diffusion and surface diffusion of impurities and point defects which lead to a local redistribution of chemical composition, mechanical stress, and electronic states. Also, electrical (ionic of electronic) charge transport in the oxide or across the oxide interfaces are known to redistribute the local electric charge density. It is obvious from these considerations that the device reliability problem is indeed a complex one.

The Program accomplishments are:

- A test pattern has been designed which can be used for life/screening test of MOS integrated circuits.

- Actual wafer lots (a total of five lots using 60 wafers) have been processed using this test pattern.

- Extensive ramp tests have been performed on the fabricated devices, which indicate, for the first time, a definitive correlation between the TDDB and the substrate type (high oxygen content Czochralski wafers or low oxygen content float zone wafers).

- A Test Method was prepared in which a failure model was proposed for use in the screening of MOS integrated circuits for time dependent dielectric breakdown. The test method is provided as an annex to the Final Report.

In Section 2, a description of the theory of TDDB is given. The test pattern and the wafer lot processing is described in Section 3. Section 4 presents the test results. Data on measurement of wafer oxygen, carbon and stress in the oxide is covered first. Then, the extensive series of ramp test data is pesented, followed by some accelerated life tests, C-V and I-V measurements and MOSFET/lateral PNP test data. Section 5 presents discussions, conclusions and recommendations.

2.0 THEORY OF TIME DEPENDENT DIELECTRIC BREAKDOWN

The Time Dependent Dielectric Breakdown (TDDB) is one of the primary causes for the gate oxide failure in MOS integrated circuits. Since the failure probability increases with increasing electric field applied to the gate oxide, the TDDB failure is more important for the thin gate oxide used in scaled down VLSI and submicron structures.

For a group of identical MOS devices (statistical sample), the time-to-fail often has a log-normal distribution [2], even though this has been questioned [1]. From the device point of view, the main task in TDDB is to predict the time-to-fail at a given percentile fail of the population and to screen out those defective parts in advance based on the results of a pre-run test which is performed within a time period shorter than the use life of the device by many orders of magnitude. There are two common methods for this, namely, the ramp test and the accelerated life test.

2.1 ACCELERATED LIFE TEST

The accelerated life test provides a physical picture more directly than the ramp test, if the correct mechanism of the failure mode is known. Regardless of the type of the distribution, whether it is a log-normal or something else, it has been found experimentally that the failure probability increases with increasing temperature and electrical field applied to the gate oxide. This experimental observation makes it possible to accelerate the failure rate drastically in the accelerated life test. The accelerated life test requires the temperature and electric field be much higher than those at the device use condition. It has been experimentally found that the time-to-fail $t(T,E)$, at a given temperature T and at a given electric field E can be expressed by

$$t(T,E) = C\exp\{(Q/kT)-aE\} \qquad (2\text{-}1)$$

where Q is the activation energy for the thermally activated failure process, k the Boltzman constant, C and a are constants [3]. The validity of this empirical expression implies that the failure mode is a thermally activated process with a single activation energy. This may not be the case if one considers the complexity of the breakdown failure mode and the rather limited temperature range (25°C-200°C) used in most experiments. Furthermore, the temperature-dependent and the field-dependent parts may not be separable as expressed in Eq. (2-1) but instead coupled; an example of the coupling appears in the form of the temperature dependency of the constant a [1]. Nevertheless, Eq. (2-1) is presently the only available explicit expression which enables one to make a quantitative extrapolation from the accelerated life to the use life in the accelerated life test technique.

From Eq. (2-1), the use life is related to the accelerated life as shown in the following expression

$$t_u = t_a A_T A_F \qquad (2\text{-}2)$$

where the temperature acceleration factor A_T and the field acceleration factor A_F are given by

$$A_T = \exp\left[\frac{Q}{k}\left(\frac{1}{T_u} - \frac{1}{T_a}\right)\right] \qquad (2\text{-}3)$$

$$A_F = \exp\{-a(E_u - E_a)\} \qquad (2\text{-}4)$$

The subscripts "u" and "a" denote the use condition and the acceleration condition respectively. The published values of both the temperature acceleration factor and the field acceleration factor range widely, probably indicating deficiency in the simple expression as Eq. (2-1). The reported value of the activation energy ranges from 0.3 ev to 2 ev [3]. The reported value of the field acceleration factor A_F also varies from 3 decade/MV/cm to 5.6 decade/MV/cm [2,3,4] and furthermore is temperature dependent [1]. It is worthy of noting that the acceleration by the electric field is far more efficient than the temperature acceleration in the normal experimental condition.

Because of the inaccurate values for the acceleration factors and undefined failure mechanisms, the results of the life prediction and screen based on the accelerated test may involve a large error. The effect of high field stress on the survived population further complicates the situation.

2.2 RAMP TECHNIQUE

Berman [1] has shown that the ramp test is more widely applicable and efficient than the accelerated life test for the life prediction and screening. He has shown that the failure vs. the electric field plot in the ramp histogram is equivalent to the failure vs. time curve in the life test. His only assumption as a starting point in the interpretation of the ramp test is an exponential dependence of the time t for any given fractional loss F on the applied field E, i.e.,

$$\left| \frac{\partial(\ln t)}{\partial E} \right|_F = -\gamma E \qquad (2\text{-}5)$$

By integrating, one gets

$$\ln t = b(F) - \gamma E \qquad (2\text{-}6)$$

where the integration constant b(F) can be interpreted as the inverse distribution function. By weighting the time spent at lower fields by the probability of failure (exponential in $-\gamma E$) and integrating, he has shown, for the staircase ramping, that the effective dwell time at a given field is related to the field as

$$t_0 = \Delta\tau \sum_{n=0}^{E_0/\Delta E} \exp\{\gamma(n\Delta E - E_0)\}$$

$$= \frac{\Delta\tau}{1-e^{-\gamma\Delta E}}$$

$$= \frac{1}{\gamma R} \qquad \text{for } \gamma\Delta E \ll 1 \qquad (2\text{-}6)$$

and independent of field if $\gamma\Delta E$ is small, where $\Delta\tau$ is the actual dwell time, ΔE is the field step. From these arguments, he has shown that the use life t(F) at a given fractional failure F can be predicted in a ramp histogram as

$$\ln t(F) = \ln t_0 + \gamma(E(F) - E_u) \qquad (2\text{-}7)$$

where E(F) is the ramp field corresponding to the fractional failure F and E_u the use electric field. The screening procedure then becomes relatively simple, i.e., one can subject the whole device population to stressing at a given maximum voltage time which corresponds to a life time at a desired fractional failure. Even though this method is fast and minimizes the screening effects on the surviving population, its validity critically depends on the assumption of Eq. (2-5) and the correct value of γ.

2.3 MECHANISMS OF TDDB

The mechanism of the TDDB is not well understood yet. Aside from the purely random statistical nature of the distribution of the time-to-fail, actual physical processes are responsible for the time dependency of each individual device. The question is whether the distribution of life-time is purely statistical or the result of an actual physical change within the device.

Various mechanisms of TDDB have been reported in the literature. Li and Maserjian [5] have considered the metallic ion diffusion to the Si-SiO_2 interface. According to this theory, the metallic ions are emitted at the gate electrode when biassed positively, subsequently diffuse in the gate oxide toward the interface region and segregate. The aggregates of these metallic ions lower the barrier height for the electrons, initiating the dielectric breakdown process at a lower field. They have contended that the time dependency of TDDB is due to the segregation kinetics of the metallic ions, mainly the sodium ions, at the silicon-oxide interface and have come up with an explicit expression for the life time prediction. The contamination of thin gate oxide by other impurities such as copper weakens the breakdown strength. [6,7]

Microdefects such as silicon inclusion, stacking fault related defects, micropores are also known to induce a premature breakdown. Other causes such as silicon-oxide interface stress, substrate effects are also suspected. For the very thin gate oxide in submicron VLSI, charge injection through a direct Fowler-Nordheim tunneling mechanism is responsible for the TDDB. The charge injected and trapped at the interface region results in a space charge region where the local field intensity is much higher than the applied average field in the gate oxide, thus initiating a premature breakdown. The time dependency in this mechanism arises from the integration time of the injection current which may range from near zero to years.

Since there are many mechanisms involved in the dielectric failure of the gate oxide, it is not surprising that life time prediction and screening results reported are indeed complex and sometimes conflicting.

3.0 TEST STRUCTURE, DEVICE PROCESSING, AND PACKAGING

A test structure was designed and a series of photo-masks were made for this program. The test pattern consists of MOS capacitors of various sizes, MOSFETs with various channel lengths, and lateral bipolar transistors having various base widths. Using this mask series, a total of five wafer lots have been processed to fabricate devices for electrical tests, each lot consisting of 12 wafers. Three types of wafers were used, n-type float zone, n-type Czochralski wafers, and p-type Czochralski. Each 12-wafer lot contained four wafers of three different types. The size of all the wafers used in this work was three inches in diameter and 20 mils in thickness. Each processed wafer had about 40 identical chips. Some of the chips were packaged in a 40-pin DIP package for electrical tests at elevated temperature.

3.1 TEST STRUCTURE

The test structure consisted of three types of devices; MOS capacitors, MOS transistors, and lateral bipolar transistors. A total of (20) MOS capacitors, 20 MOSFETs, and 20 bipolar transistors were designed on the test pattern using 2-micrometer (μm) design rules. Table 3-1 lists all the devices and their dimensions. A total of seven NBS 40-pin bonding pad sets were included in the test pattern for electrical connections. Figure 3.1 shows the test pattern. A body or substrate contact is provided for each device.

The capacitor size and shape varies from 50μm x 1000μm to 3000μm x 3333μm. Among these capacitors, a set of ten standard square capacitors of a 1000μm x 1000μm size has been used primarily for the electrical tests. The long, narrow capacitors were designed particularly for testing the expected enhanced dielectric breakdown events at the capacitor perimeters.

All of the MOSFETs in the test pattern have a fixed channel width of 40μm. The channel length varies from 1μm to 20μm. Figure 3.2 shows a typical MOSFET. The lateral bipolar transistors are structurally similar to the MOSFETs, namely the gate is used as a field plate and the channel region is used as the base region. The only difference is in that the MOSFET has a straight open-ended shape while the bipolar transistor has a closed square

Table 3-1. List of Devices in the Test Pattern

MOS Capacitors:

Size (μm^2)	Number
1000x1000	10
3333x3000	1
3000x2000	1
2000x2000	1
4000x1000	1
4000x500	1
4000x250	1
4000x125	1
2000x1000	1
2000x500	1
2000x250	1
2000x125	1
16300x100	1
8300x100	1
4100x100	1
4050x50	1
8150x50	1
12250x50	1

MOSFETs:

Channel Length (μm)	Channel Width (μm)	NO.
20	40	2
15	40	2
10	40	2
8	40	2
5	40	2
4	40	2
3	40	2
2	40	2
1.5	40	2
1	40	2

Bipolar Transistors:

Base Width (μm)	Base Length (μm)	NO.
10	80	2
9	80	2
8	80	2
7	80	2
6	80	2
5	80	2
4	80	2
3	80	2
2	80	2
1	80	2

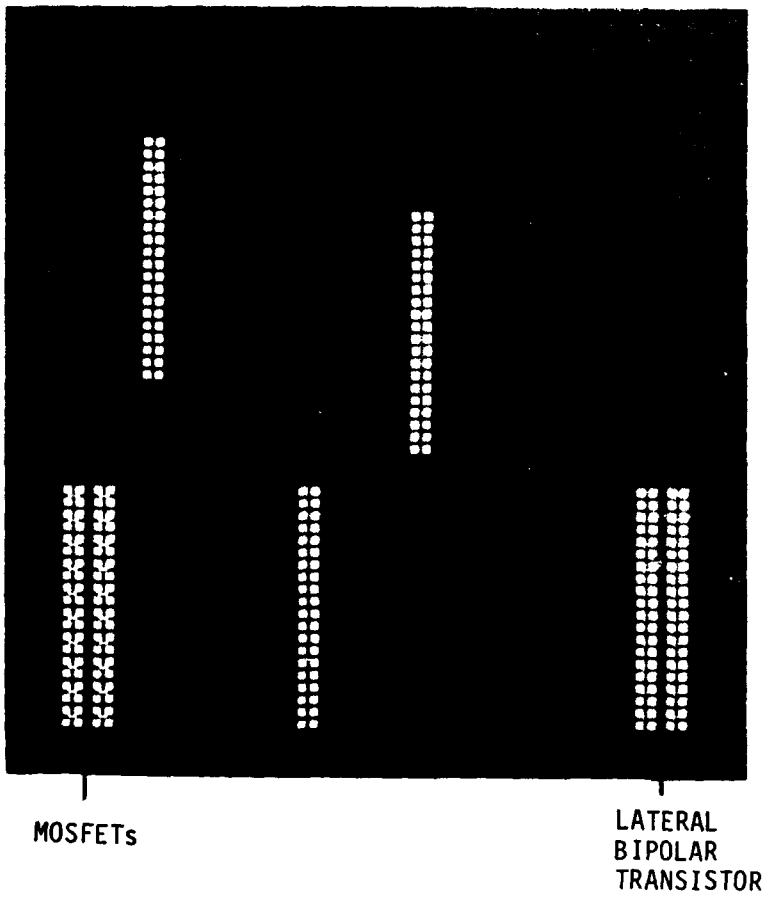


Figure 3.1 Test Pattern

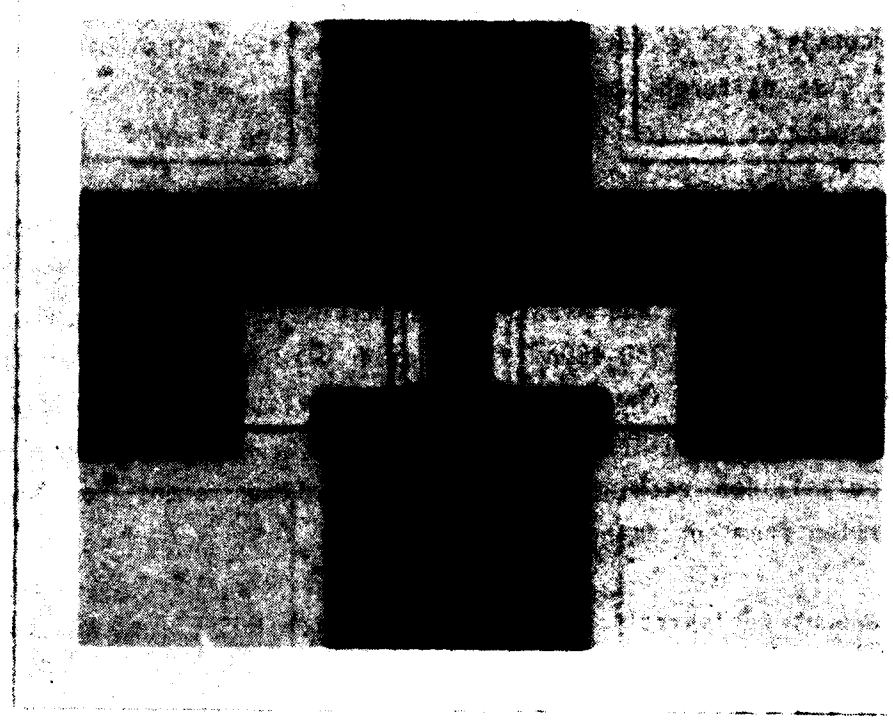


Figure 3.2 Picture of a Typical MOSFET

wall-shaped field plate. Figure 3.3 shows a typical bipolar transistor in the test pattern.

3.2 WAFER PROCESSING (DEVICE FABRICATION)

A total of five lots (#5739, #5826, #5832, #5833, and #5878), each consisting of 12 3-inch wafers, were processed using part of the Westinghouse CMOS processing technology. Three lots (#5739, #5832, and #5878) were used to fabricate p-channel MOS devices and the remaining two lots (#5826 and #5833) for n-channel device processing. Table 3-2 shows the lot-wafer matrix. The processing consists of a total of 26 processing steps including seven photo steps using five different photo-masks and six ion implant steps. Table 3-3 shows an overview of the lot status and key processing steps.

For all the lots processed, N^+-polysilicon as gate electrode, dry oxide for the gate dielectric, wet oxide for the field oxide, and Silox for isolation of metal lines, and Al/Si for metallization were employed. The gate oxide was grown after a 350-400nm field oxide was etched away in the active device area to eliminate the bird beak or Kooi effect. For the first and the last lots (#5739 and #5878), a 20nm LPCVD nitride was overlayed immediately after the polysilicon etching step (gate definition step) for better gate oxide protection from contamination.

The dopant concentration at the body of the MOSFET, at the base region of the bipolar transistor, and under the gate electrode of the MOS capacitor was determined primarily by a single ion implant (phosphorous, $1x10^{13}$ @ 190kev for p-channel device lots; boron, $1x10^{13}$ @ 80kev for the n-channel device lots) followed by a drive-in anneal (8 hours @ 1150C). A SUPREM run gives a value of $8x10^{16}/cm^3$ with a junction depth of about 2μm. This implant and drive-in anneal process provided a 2μm thick layer of n or p region depending on the combination of the lot type and wafer type. The p-n junctions 2μm below the wafer surface were absent for some wafers. Westinghouse submicron device processing uses this same implant in conjunction with a threshold adjust implant. Since we are not interested in threshold adjust in this work, we have eliminated the threshold adjust implant step.

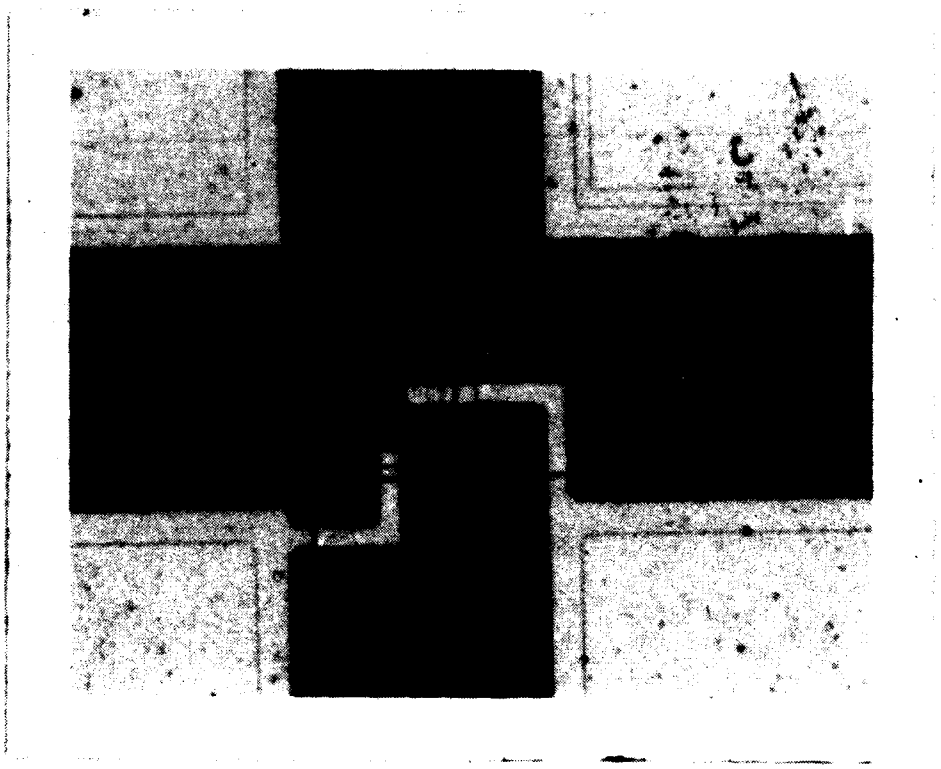


Figure 3.3 Picture of a Typical Bipolar Transistor

Table 3-2. Wafer Allocation

Wafer Type / Lot #	Float Zone N-Type	Czochralski N-Type	Czochralski P-Type
5739 (PMOS)	0	12	0
5826 (NMOS)	4	4	4
5832 (PMOS)	4	4	4
5833 (NMOS)	4	4	4
5878 (PMOS)	4	4	4

Table 3-3. Key Process Steps

Steps \ Lot #	5739	5826	5832	5833	5878
Body Implant	(Ph) $1x10^{13}$/190kev thru 34.0nm oxide	(B) $1x10^{13}$ @ 80kev thru 28.2nm oxide	(Ph) $1x10^{13}$ @ 190kev 21.7nm oxide	(B) $1x10^{13}$ 60kev thru 20.0nm oxide	(Ph) $1x10^{13}$/190kev thru 20.0nm oxide
Drive-in Anneal	1150°C-8HR (186Ω/□)	1150°C-8HR	1150°C-8HR X_1 = 3.6μm	1150°C-8HR	1150°C-8HR X_1 = 2.45μm
Field Oxide	1000° 580nm	1000°C-120min 370nm	1000°C-120min 370nm	1000°C-100min 330nm	1000°C-100min 330nm
Gate Oxide	900°C-135min Dry O_2/Anneal X_{ox} = 33.9nm	Dry O_2/Anneal X_{ox} = 33.8nm	Dry O_2/Anneal X_{ox} = 36.8nm	Dry O_2/Anneal X_{ox} = 19.8nm	Dry O_2/Anneal X_{ox} = 21.1nm
Polysilicon	609.9nm 23.4Ω/□	611.1nm 15.8Ω/□	611.3nmm 15.8Ω/□	650.0nm 9.7Ω/□	620.0nm 13.2Ω/□
Source-Drain Implant	(BF2) $1.4x10^{15}$ 80kev thru 33.9nm Oxide	(As) $1.4x10^{15}$ 80kev thru 33.8nm Oxide	(BF2) $1.4x10^{15}$ @ 80kev thru 36.8nm Oxide	(As) $1.4x10^{15}$ 80kev thru 20.0nm Oxide	(BF2) $1.4x10^{15}$ 80kev thru 20.0nm Oxide
LPCVD Nitride	20.0nm	None	None	None	20.0nm
Silox	Silox 370nm	Silox 350nm	Silox 390nm	Silox 350nm	Silox 350nm
Reflow	900°C-30 Min	900°C-30 Min	900°C-30 Min	900°C-30 Min	900°C-30 Min
Source-Drain Contact Implant	(B) $4x10^{14}$ 80kev (B) $4x10^{13}$ 140kev	(Ph) $2x10^{15}$ 70kev (bare) (Ph) $2x10^{14}$ 140kev	(B) $4x10^{14}$ @ 80kev (B) $4x10^{13}$ 140kev	(Ph) $2x10^{15}$ 70kev (Ph) 2x1014-140kev	(B) $4x10^{14}$ 80kev (B) $4x10^{13}$ 140kev
Body Contact Implant	(Ph) $2x10^{15}$ 70kev (Ph) $2x10^{14}$ 140kev	(B) $4x10^{14}$ 80kev (Ph) $4x10^{13}$ 140kev	(Ph)$2x10^{15}$ 70kev (Ph)$2x10^{14}$ 140kev	(B) $4x10^{14}$ 80kev (B) $4x10^{13}$ 140kev	(Ph)$2x10^{15}$ 70kev (Ph)$2x10^{14}$ 140kev
Anneal	900°C-30 Min N_2	900°C-30 Min N_2	900°C-30 min N_2	900°C-30 min N_2	900°C-30 Min N_2
Metal-lization	Al/Si 700nm	Al/Si 720nm	Al/Si 720nm	Al/Si 750nm	Al/Si 760nm

For the drain-source (or emitter and collector), a single shallow implant through the gate oxide was employed (arsenic $1.4x10^{15}$ @ 80kev for the n-channel device lots; BF_2, $1.4x10^{15}$ @ 80Kev for the p-channel lots). For contacts to the drain and to the source (or emitter and collector), two successive implants through the contact window placed in the region away from the gate region were employed (boron, $4x10^{14}$ @ 80kev and $4x10^{13}$ @ 140kev for the p-channel lots; phosphorous, $2x10^{15}$ @ 70kev and $2x10^{14}$ @ 140kev for the n-channel lots). The same implants provided for the contact to the body (or base) for the lots of opposite sign. These implants were followed by an activation anneal (30 min. @ 900°C in N_2 gas).

The gate oxide was grown in dry O_2 gas at 900C followed by a 30min-900C anneal in argon gas. The thickness of the gate oxide was measured by a Rudolph ellipsometer, and rechecked by C-V measurements after the fabrication process was completed. The thickness of the gate oxide ranged from 18.0nm to 40.0nm. TBS measurements showed a mobile ion density $<10^{10}/cm^2$. The typical value of gate oxide thickness for each lot is included in Table 3-3. Figure 3.4 shows a picture of the processed wafer.

3.3 PACKAGING

About 40 chips were bonded and packaged in a 40-pin DIP package without hermetic sealing for electrical tests, primarily for accelerated life test at elevated temperature. Figure 3.5 shows a picture of the packaged chip. The destructive ramp tests were performed using a whole wafer.

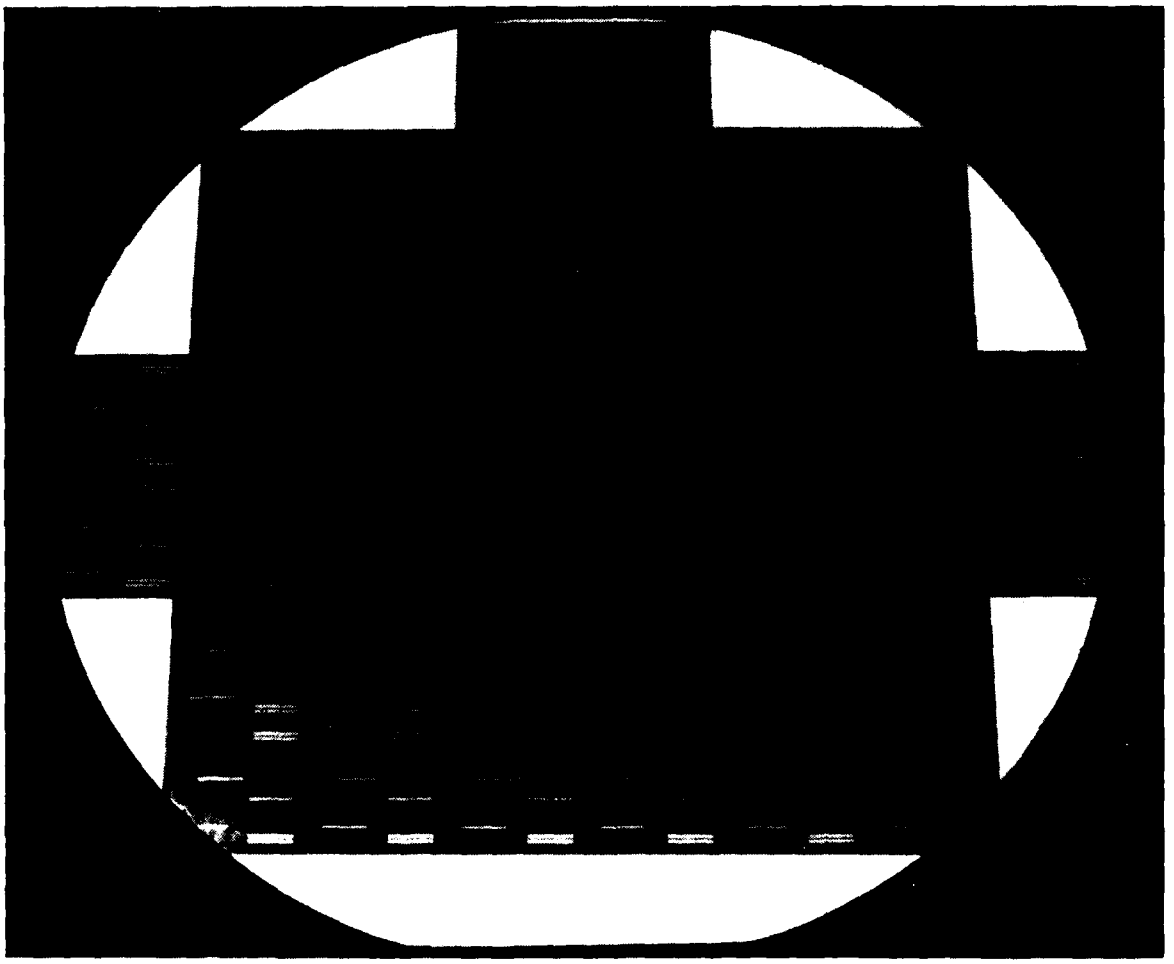


Figure 3.4 Picture of a Processed Wafer

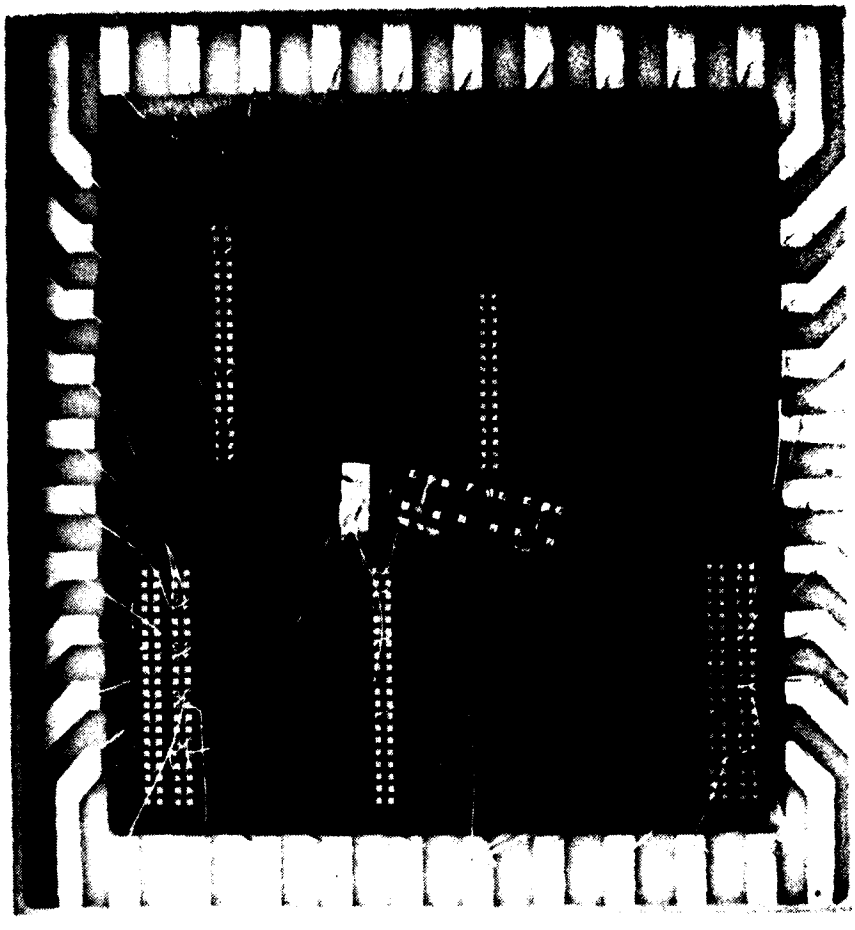


Figure 3.5 Picture of a Packaged Chip

4.0 TESTS AND RESULTS

One of the main objectives of the electrical measurements in this work was to examine the effects of various parameters such as oxygen impurity content of the silicon substrate, the thickness of the gate oxide, the oxide growth condition, the mechanical stress at the $Si-SiO_2$ interface on the time dependent dielectric breakdown failure of silicon MOS devices. From the results in the open literature in conjunction with our results, a practical model for TDDB failure was to be constructed, and a test procedure was to be devised for device life prediction and screening of defective parts.

We have made extensive room temperature ramp tests for each representative of the fabricated MOS capacitors. The results of this test indicate a definitive correlation between the TDDB failure and the type of the substrate used as the starting material as well as the oxide thickness, as will be seen later in this chapter. A preliminary life test at an accelerated condition has been performed on selected MOS capacitors in order to obtain a reference failure vs. time curve from which, with values of acceleration factors reported in the literature, the use life of the device can be extrapolated. In the threshold voltage shift and the sub-threshold leakage current of selected p-channel MOSFETs at room temperature and at an elevated temperature under an electrical bias condition have been measured. The results of these measurements and I-V measurements on MOS capacitors, which show interesting structures, will be presented in this section.

4.1 WAFER TESTS

4.1.1 OXYGEN CONCENTRATION

The interstitial oxygen concentration was measured on selected wafers. The wafers purchased for this study were received at the Research & Development Center in trays containing 25 wafers each. The wafers at each end of the tray, and the wafer at the center, were removed for characterization, while the remaining 22 wafers in each tray were sent to ATL for processing. Retained wafers were labelled according to their origin and submitted for oxygen determination without any processing or preparation.

Oxygen determinations were carried out by the method of infrared absorption. Each wafer was mounted in a Nicolet model 7000 Fourier Transform Infra Red (FTIR) spectrometer for measurement of the magnitude of the oxygen absorption peak at 1105 cm^{-1} The infrared beam diameter is about 3 mm, located at the center of the wafer. The background silicon absorption was subtracted by using a purified silicon wafer as a reference standard. The reference wafer was a float-zone sample that had been subjected to six-pass zone refining and had been characterized for extremely low levels of oxygen and carbon. The Nicolet instrument utilizes digital signal acquisition and data storage for drift-free long term signal averaging. The stored data was analyzed using the built-in data processing capability of the Nicolet to subtract the interference fringes due to sample and reference wafer thickness, to subtract the silicon baseline, and to compute the absorbance at the oxygen peak. Absorbance A is defined as

$$A = \log I_o/I_t$$

where I_t is the transmitted intensity at the wavelength of the oxygen peak, and I_o is the incident intensity. Since the intensity decreases by 10 percent or less for the 500 micron thick wafers to be characterized, an accurate, stable system is necessary to obtain reliable data. The absorbance is related to the absorption coefficient α by

$$\alpha = \frac{1}{t} \ln \frac{I_o}{I_t} = \frac{2.30A}{t}$$

where t is the sample thickness in cm. The thickness t is taken as 508 micrometers, which corresponds to the nominal 20 mil thickness specification of the wafers. The thickness was checked on selected wafers by mechanical measurement and by the interference fringe pattern observed in the FTIR measurements. The thickness was within 10 micrometers of nominal, giving a maximum two percent error in α due to neglecting this source of variation.

There is still some debate over the correct calibration relating interstitial oxygen concentration to the absorption coefficient. Accordingly, the data are analyzed both by the new ASTM standard (F121-80) and the old ASTM standard. The calibration coefficients are shown in Table 4-1. Ten wafers of

Table 4-1. Calibration Coefficient for Interstitial Oxygen Concentration

Calibration	[O] ppma	[O] cm^{-3}
New ASTM	4.9 α	2.45 α x 10^{17}
Old ASTM	9.63 α	4.82 α x 10^{17}

each variety were measured. The float-zone wafers showed no detectable oxygen peak. The sensitivity limit is estimated at 0.0012 absorbance (0.53 ppma or 2.8×10^{16} by old ASTM standard) by the noise level observed on the FTIR spectra. This is consistent with the expected low concentration typical of float-zone material. The data for the Czochralski (Cz) wafers are shown in Table 4-2.

The data may be analyzed as follows. Within each group, the data are tightly clustered. In each case, the rms variation in the absorbance is close to the estimated noise level; the rms variation for pCz is 0.0013, for nCz is 0.0012, and the estimated noise level is 0.0012. Thus, there is no statistically significant variation of oxygen concentration among wafers within each group, at the present level of accuracy of the measurement. This implies minimal axial variation in oxygen in the silicon boule, so that wafers cut from the same boule will consistently have the same oxygen content.

The oxygen content of the pCz group is different from that of the nCz group, but the difference is not as large as expected. The difference of the mean values of absorbance is 0.0083, while the sum of the rms variations on the two groups is 0.0025. The difference of means is 3.3 times the sum of variations, strongly indicating that the difference in oxygen concentrations is statistically significant. The difference is smaller than expected based on the specifications and typical values obtained from the vendor at the time of ordering. According to the vendor, the typical oxygen concentration for the medium oxygen grade pCz wafers was 26, with a specification range from 23 to 35, in the old ASTM calibration. As shown in Figure 4.1, the wafers we measured have a mean oxygen level of 33.5, at the high end of the specification range. The high oxygen nCz wafers have a mean oxygen level of 37.2, close to the typical value of 36 for that grades. As Figure 4.1 shows, there is considerable overlap in the specification ranges of all grades, so that even the medium oxygen and very high oxygen grades overlap. This reflects the situation in the degree of control of oxygen incorporation in Czochralski crystal growth at the time the order was placed.

Table 4-2. Oxygen Concentration Data

1. pCz Wafers of Medium Oxygen Grade

Sample No.	Absorbence	Absorption Coefficient cm^{-1}	New ASTM Calibration ppma	New ASTM Calibration cm^{-3}	Old ASTM Calibration ppma	Old ASTM Calibration cm^{-3}
213	0.0750	3.399	16.65	8.33E17	32.73	1.64E18
231	0.0754	3.418	16.75	8.37E17	32.91	1.65E18
233	0.0757	3.427	16.79	8.40E17	33.00	1.65E18
211	0.0766	3.469	17.00	8.50E17	33.40	1.67E18
221	0.0769	3.482	17.06	8.53E17	33.54	1.68E18
241	0.0769	3.484	17.07	8.54E17	33.55	1.68E18
212	0.0770	3.489	17.10	8.55E17	33.60	1.68E18
222	0.0775	3.513	17.21	8.61E17	33.83	1.69E18
223	0.0786	3.560	17.44	8.72E17	34.28	1.71E18
232	0.0792	3.589	17.58	8.79E17	34.56	1.73E18
		Statistical Summary				
High	0.0792	3.589	17.58	8.79E17	34.56	1.73E18
Low	0.0750	3.399	16.65	8.33E17	32.73	1.64E18
Mean	0.0769	3.483	17.07	8.53E17	33.54	1.68E18
rms	0.0013	0.057	0.28	1.40E16	0.55	2.75E16

2. nCz Wafers of High Oxygen Grade

Sample No.	Absorbance	Absorption Coefficient cm^{-1}	New ASTM Calibration ppma	New ASTM Calibration cm^{-3}	Old ASTM Calibration ppma	Old ASTM Calibration cm^{-3}
311	0.0824	3.733	18.29	9.15E17	35.95	1.80E18
323	0.0842	3.815	18.70	9.35E17	36.74	1.84E18
312	0.0845	3.826	18.75	9.37E17	36.84	1.84E18
322	0.0853	3.863	18.93	9.46E17	37.20	1.86E18
333	0.0856	3.877	19.00	9.50E17	37.34	1.87E18
331	0.0857	3.882	19.02	9.51E17	37.38	1.87E18
341	0.0857	3.882	19.02	9.51E17	37.38	1.87E18
313	0.0859	3.891	19.07	9.53E17	37.47	1.87E18
321	0.0859	3.891	19.07	9.53E17	37.47	1.87E18
322	0.0869	3.939	19.30	9.65E17	37.93	1.90E18
		Statistical Summary				
High	0.0869	3.939	19.30	9.65E17	37.93	1.90E18
Low	0.0824	3.733	18.29	9.15E17	35.95	1.80E18
Mean	0.0852	3.860	18.91	9.46E17	37.17	1.86E18
rms	0.0012	0.053	0.26	1.31E16	0.51	2.57E16

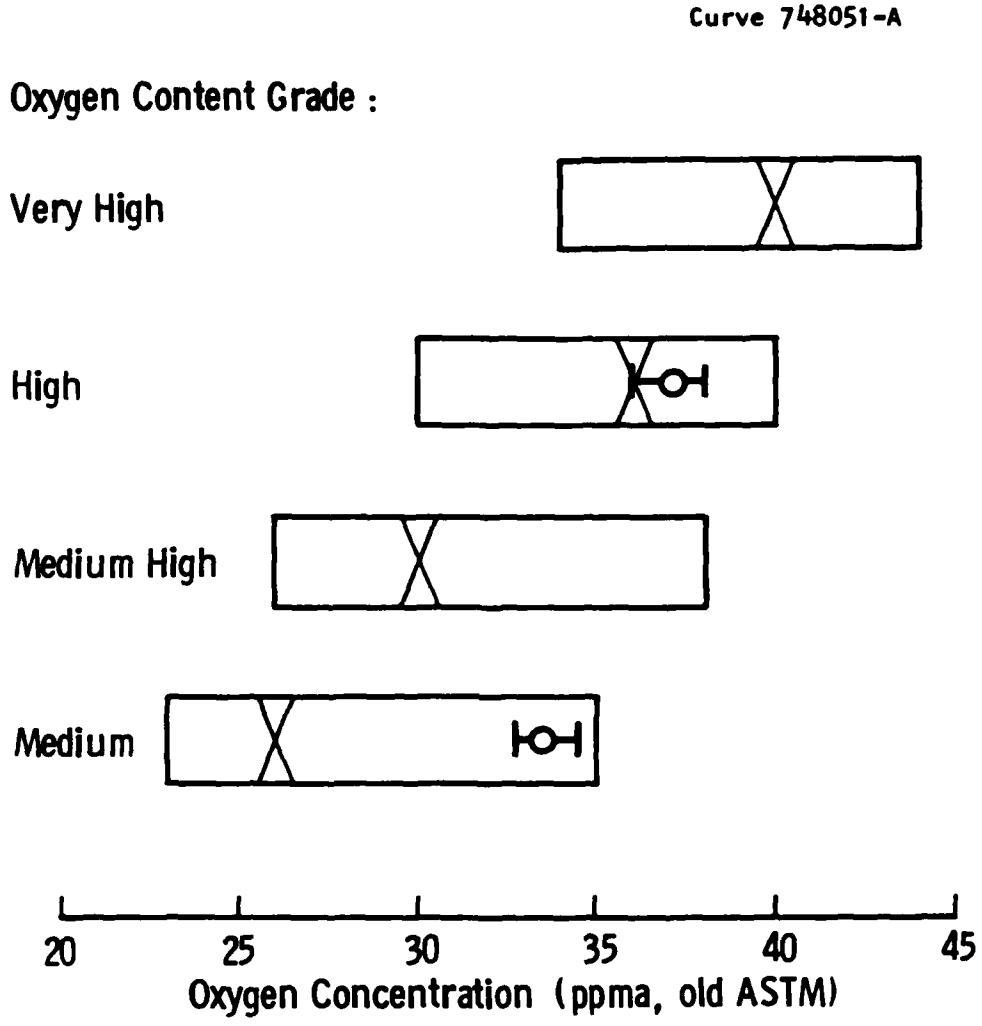


Figure 4.1 Measured oxygen content compared to vendor specifications at time of order. The specification range for each grade is shown as open box, with the expected typical value shown by an X. The Westinghouse data is displayed as a heavy bar indicating the range of values measured in 10 wafers of each of the two grades purchased, while the mean value is shown as a circle.

4.1.2 OXYGEN PROFILES

The oxygen concentration was measured as a function of position in sample wafers of both Czochralski oxygen grades. Float-zone wafers were omitted since the oxygen concentration was below the detection limit. Each wafer was placed in a sample holder with a calibrated position slide. The FTIR oxygen determination was repeated following translations of the sample by 10 mm intervals in both directions away from the center. The wafer was rotated in the holder to allow mapping along two orthogonal axes. The beam size was about 3 mm at the sample. The spatial resolution imposed by the beam diameter was not sufficient to attempt to look for microscale variations, but was adequate to characterize larger scale variations in oxygen content.

The results for a pCz wafer of medium oxygen grade are shown in Figure 4.2. The profiles along both axes are non-uniform, dropping sharply near the rim of the wafer. The last data points on each axis are still 8 mm from the edge, within the nominally good processing area of the wafer. As seen in Table 4.2, the rms variation in the oxygen content at the centers of 10 wafers of this type was 0.55 ppma in old ASTM calibration, which approximately equals the noise level in the measurement. The variation along a diameter is about six times as great as the variation between wafers at the center.

The measurements from an nCz wafer of high oxygen grade are shown in Figure 4.3. All of the data points are within 0.5 ppma of the mean, and so there is no statistically significant variation in the oxygen content of this wafer as a function of position.

4.1.3 CARBON CONCENTRATION

The carbon determinations were done by the FTIR method described for oxygen determination. The carbon absorption peak at 605 cm^{-1} coincides with silicon absorption peaks. Because of this interference, the subtraction of the background by means of a standard wafer becomes more difficult for the case of different thicknesses of standard and test wafer. The calibration for carbon concentration is taken as the ASTM F123-81 standard

$$[C] = 2.0\alpha(ppma) = 1.0\alpha \times 10^{17}(cm^{-3})$$

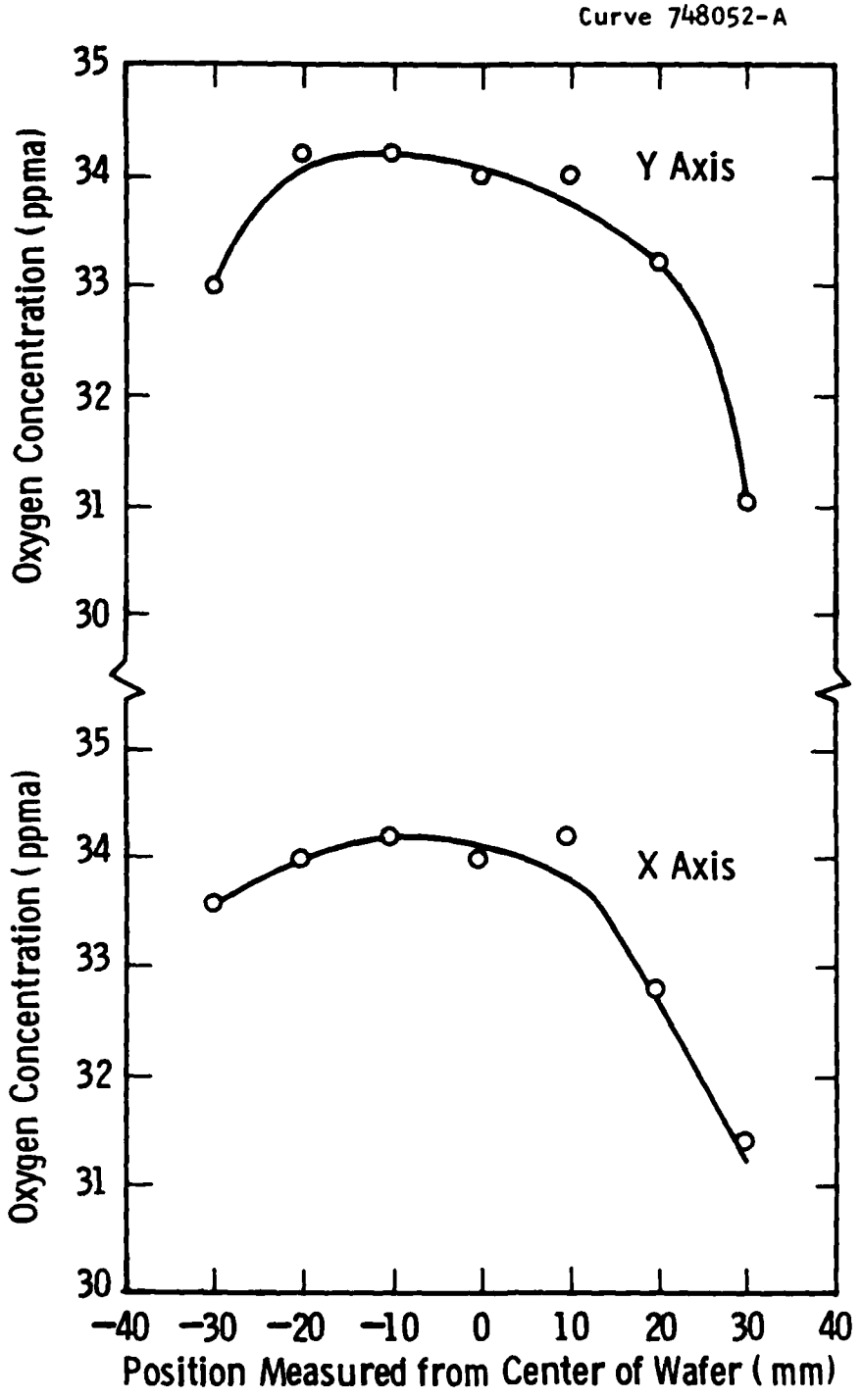


Figure 4.2 Oxygen profiles for pCz wafer of medium oxygen grade. The data are given in the old ASTM calibration.

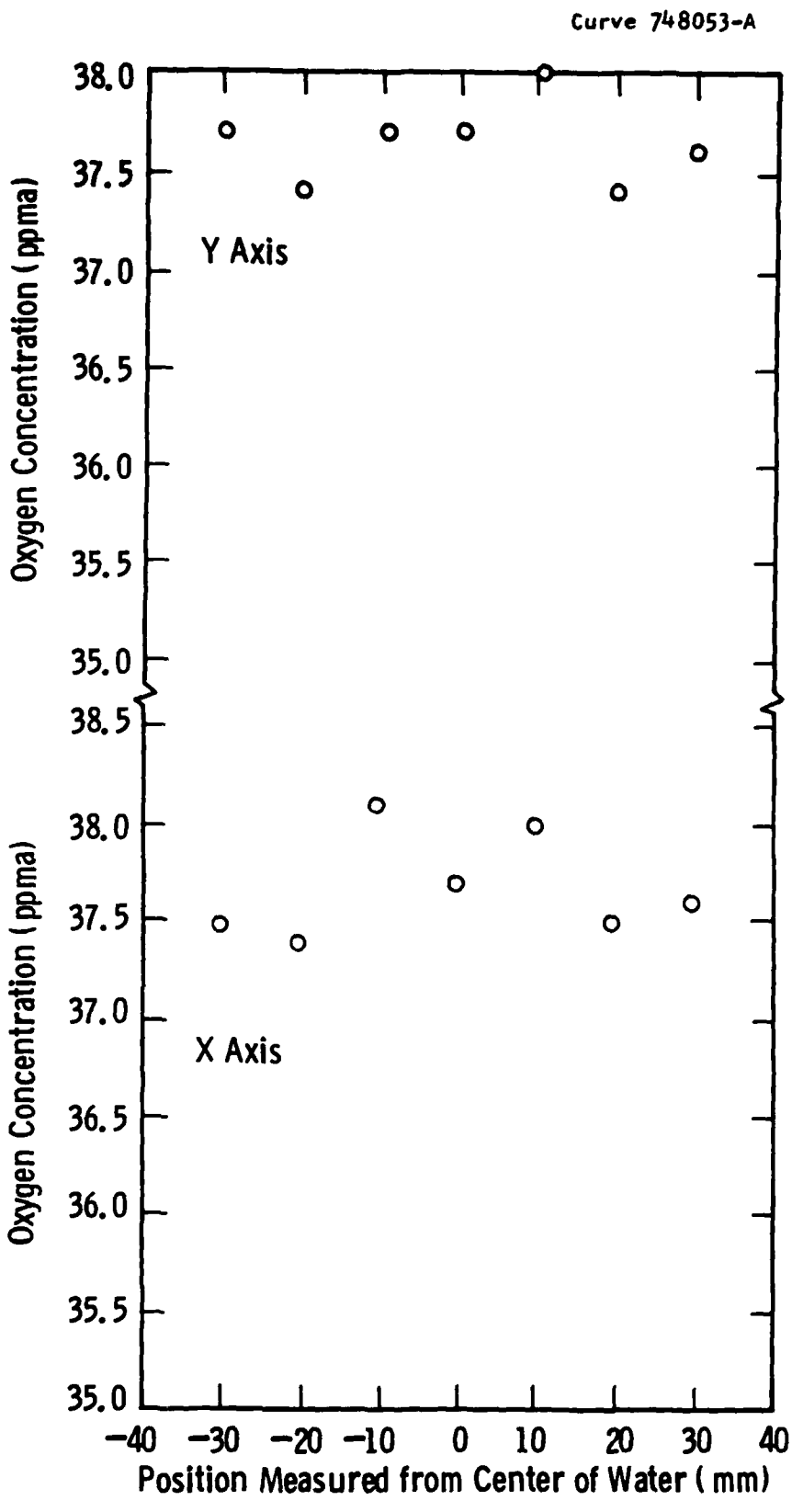


Figure 4.3 Oxygen profiles for nCz wafer of high oxygen grade. The data are given in the old ASTM calibration.

Wafers of each of the types (float zone, PCz medium oxygen, and nCz high oxygen) were characterized for carbon content at room temperature. The carbon peak was not detectable in any of the samples. Some difficulty was encountered in getting good subtraction of the silicon lattice bands due to the difference in thickness between the test sample (.5 mm) and the reference sample (1.57 mm). A further attempt was made to get a definite carbon reading by preparing samples for low temperature measurement. Discs about 23 mm in diameter were cut from the 3-inch wafers to fit into a cryostat. Samples were inserted and cooled to 77 K using liquid nitrogen. The cooling was expected to reduce the amplitude of the silicon lattice bands. However, the carbon band was still not detectable.

4.1.4 DLTS MEASUREMENTS

Completely fabricated test samples on float-zone, pCz medium oxygen grade, and nCz high oxygen grade substrates were selected for DLTS measurements. The objective was to characterize the silicon substrate near the surface for deep level traps that would indicate the presence of impurities, residual damage, or defects. The test samples contained MOS capacitors of various areas, adjacent to capacitors that had been breakdown tested. The test samples were cut into small chips and mounted on headers, with wires bonded from the contact pads on the chip to the header pinouts. The headers were inserted in the DLTS system sample holders for cooling to 77°K during the DLTS runs.

The initial measurements were obscured by spurious peaks that were not reproducible. These effects were traced to two causes. First, the capacitor bias was originally set in deep depletion. The capacitance recovery as the inversion formed gave large spurious responses. This effect was eliminated by reducing the baseline capacitor bias to avoid deep depletion. The second source of spurious response was traced to moisture accumulating on the sample surface. Although the samples were mounted in a sealed enclosure, the headers holding the sample chips were not covered leaving the samples open to the atmosphere in the enclosure. As a result, the moisture condensing on the sample varied the resistivity of the poly, causing difficulty in getting a steady capacitance reading. This problem was minimized by heating the sample to about 80°C to drive off moisture while the sample chamber is surrounded by

nitrogen vapor above the liquid nitrogen cooling bath. The heating current is then turned down gradually and the sample cools in a dry environment, minimizing the accumulation of moisture.

By taking these precautions, DLTS curves were taken on samples from the three grades of silicon substrates with 20 nm and 34 nm oxide thickness. No peaks were observed on any of the samples. The detection limit on the density of deep levels is about 1000X below the carrier density in the region near the surface. The surface concentration is about 10^{17} cm^{-3}, giving a upper limit on electrically active deep level traps of about 10^{14} cm^{-3}.

4.1.5 OXIDE STRESS

The samples for stress measurement were subject to normal processing steps up to the growth of the gate oxide. This ensures that the stress measured in the test samples will be representative of the stress in the wafers subjected to dielectric breakdown testing. Following cleaning, a 20 nm oxide buffer layer was grown. The wafers were then implanted with boron at 60 kV to a dose of 10^{14} cm^{-2}. The implant was driven in with an 8-hour 1150°C cycle. The buffer oxide was stripped and a 600 nm field oxide was grown. At this point, the wafers for dielectric breakdown testing are patterned to define the gate area of the test devices, by opening apertures in the field oxide. For the stress samples, the entire field oxide was stripped. The gate oxide was grown, with the stress test wafers and the dielectric breakdown test wafers in the same lot. The gate oxide thickness was measured by ellipsometer to be 33.6 nm. The stress wafers were removed from the process stream at this point.

Preliminary calculations showed that the radius of curvature would be difficult to measure for the relatively thick substrate and thin oxide used for this study. Since the radius varies as the square of the substrate thickness, the stress measurement wafers were thinned to get a more readily measurable curvature. The thinning was carried out after the growth of the oxide to avoid breakage in processing of the thinner wafers. Each wafer was pressed onto a lapped carrier, using a sheet of lens paper to protect the oxide surface. Wax was used as the bonding agent to hold the wafer rigidly on the carrier. The exposed back surface of the wafer was then lapped in a Hipol

single-sided polishing machine with Nalco abrasive compound diluted in 20 parts of water, until the wafer was nominally reduced to half of the original thickness, from 500 to 250 micrometers. The wafers were then removed from the carriers by dissolving the wax in solvents. Inspection of the oxidized surface of the wafer showed no evidence of damage from this procedure.

The method of stress measurement is inference of interface stress from wafer curvature. The wafer shape was measured by two means. An optical instrument, the Tropel model 9000 wafer flatness analyzer, was used to make interferograms showing the surface conformation of the wafers under various mounting methods. Also, a high resolution double crystal X-ray monochromator was used to track the crystallographic orientation of the wafer surface over a linear scan range. These means are now described in more detail.

For the optical measurements, the wafer is suspended close to an optically flat glass surface of the Tropel machine. A laser beam is directed onto the glass surface from inside the machine, and the interference fringes generated by the closely spaced glass surface and the wafer surface, are detected by a vidicon inside the machine and displayed on a TV monitor. The fringe sensitivity is adjustable by changing the angle of incidence of the laser beam. The final display is a contour map of the surface of the wafer. A vacuum fixture is used to support the wafer in position close to the optical flat. The wafer is held about 3 degrees off from a vertical position to minimize the deformation of the wafer caused by gravity. The vacuum fixture applies vacuum to a circular region about 8 mm diameter at the center of the wafer. Aside from this support region, the wafer is unconstrained. However, the wafer fringe map can be seen to distort as the vacuum applied to the support is adjusted through its range from 6 to 25 inches of vacuum. To account for the wafer distortion caused by the vacuum, the wafer surface map was photographed with maximum (25 inches), minimum (6 inches), and no vacuum applied. For the zero vacuum case, the wafer rested on its flat on a lapped steel block pressed against the glass. The wafer touched the glass, but due to the nearly vertical position, the contact force with the glass was small and did not produce local distortion. With the wafer held by the vacuum fixture, adjustment screws could be used to eliminate tilting of the wafer with respect to the glass. Upon removing and remounting the wafer, repeatable fringe patterns could be obtained after readjusting the screws on the mounting

fixture. This facility was lost for the vacuum free case, and only by patient tweaking of the wafer could a symmetrical fringe pattern be obtained.

The problem of satisfactory support for the wafer also existed for the X-ray measurements. The wafer was mounted in a vertical position resting on edge on a shelf projecting from the sample holder. To keep the wafer in place, three small dots of soft wax were used to bond the back of the wafer to the sample holder. After mounting, the wafer was stored for several days in a temperature-controlled box to allow any residual strains to relax through viscous flow of the soft wax. Then the wafer was mounted on a linear translation stage on the goniometer of a computer-controlled double crystal monochromator. As the sample was translated in steps of about 5 mm, the goniometer was rotated to maintain the (400) Bragg peak.

The radius of curvature R near the center of a wafer that is elastically deformed by a thin surface film under stress α is given by

$$R = \frac{E\,T^2}{6(1-V)t\sigma} \qquad (4\text{-}1)$$

where E is the elastic modulus of the substrate, v is the Poisson's ratio of the substrate, T is the thickness of the substrate, and t is the thickness of the surface film [8]. This relation presupposes that the substrate is perfectly flat before the surface stress is applied. This is not the case for the silicon wafers of this study. Interferograms of wafers as received from the vendor show that the wafers are typically bowed by 5 to 10 micrometers into shapes that are roughly spherical or saddle shaped. Thus, it is necessary to observe the change in curvature caused by the oxide in order to measure the oxide stress. This was accomplished by measuring wafer curvature before and after the oxide film was etched away by dipping the wafers in HF. (The other possibility, measurement before and after oxidation, was ruled out because of the expected changes in residual stress in the substrate that would be caused by the high temperature processing). Solving equation (4-1) for σ and taking the difference of two readings,

$$\sigma_{ox} = \frac{E\,T^2}{6(1-V)t}\left(\frac{1}{R_1} - \frac{1}{R_0}\right) \qquad (4\text{-}2)$$

where R_1 is the measured radius with the oxide in place, R_0 is the radius with the oxide etched away and consequently the zero surface stress case, and σ_{ox} is the true stress in the oxide film. Once the stress in the film is known, the maximum stress σ_m in the substrate, which occurs at the surface, can be found from

$$\sigma_m = \frac{-\sigma_{ox} t}{4T} \qquad (4\text{-}3)$$

where the change in sign indicates that a compressive stress in the oxide produces a tensile stress in the silicon substrate [8].

The interferograms for the optical characterization of the float-zone wafer E4 are shown in Figure 4.4. The sample shape is concave or dished under all conditions shown. This was determined by applying finger pressure to the sample and watching the motion of the fringes. It is consistent also with the greater curvature observed when higher vacuum is applied. Assuming the wafer was perfectly flat before oxidation, the growth of a surface oxide in compression should make the wafer convex or crowned.

The distortion of the wafer caused by the vacuum chuck is evident in Figure 4.4. The central region of the wafer is most strongly affected but the overall fringe pattern also shifts. It is also clear that the wafer is non-spherical in shape, with a pronounced local projection near the bottom edge. The same local projection is visible in interferograms taken before thinning. The shape of the wafer shows that the deformation due to the stress built into the oxide is a small effect compared to residual stresses in the wafer. Comparing the interferograms before and after the oxide is etched away, it is seen that the curvature increases when this is removed. Thus, the oxide is in compression and tends to counteract the internal stresses that make the wafer concave. Removal of the oxide allows the internal stress to produce a greater curvature.

The interferograms for the pCz medium oxygen grade wafer are shown in Figure 4.5. The wafer shows an axis of symmetry of low curvature. In taking fringe counts for this wafer, the apparent axis of symmetry was taken as the X-axis. This wafer was also concave and had an increased curvature upon removing the oxide.

VACUUM APPLIED:

25"

6"

OXIDE THICKNESS: 34 NM 0

Figure 4.4 Optical Interferograms of Wafer E4 (Float Zone) Before and After the Oxide Was Etched Away, Taken Under High and Low Vacuum Conditions.

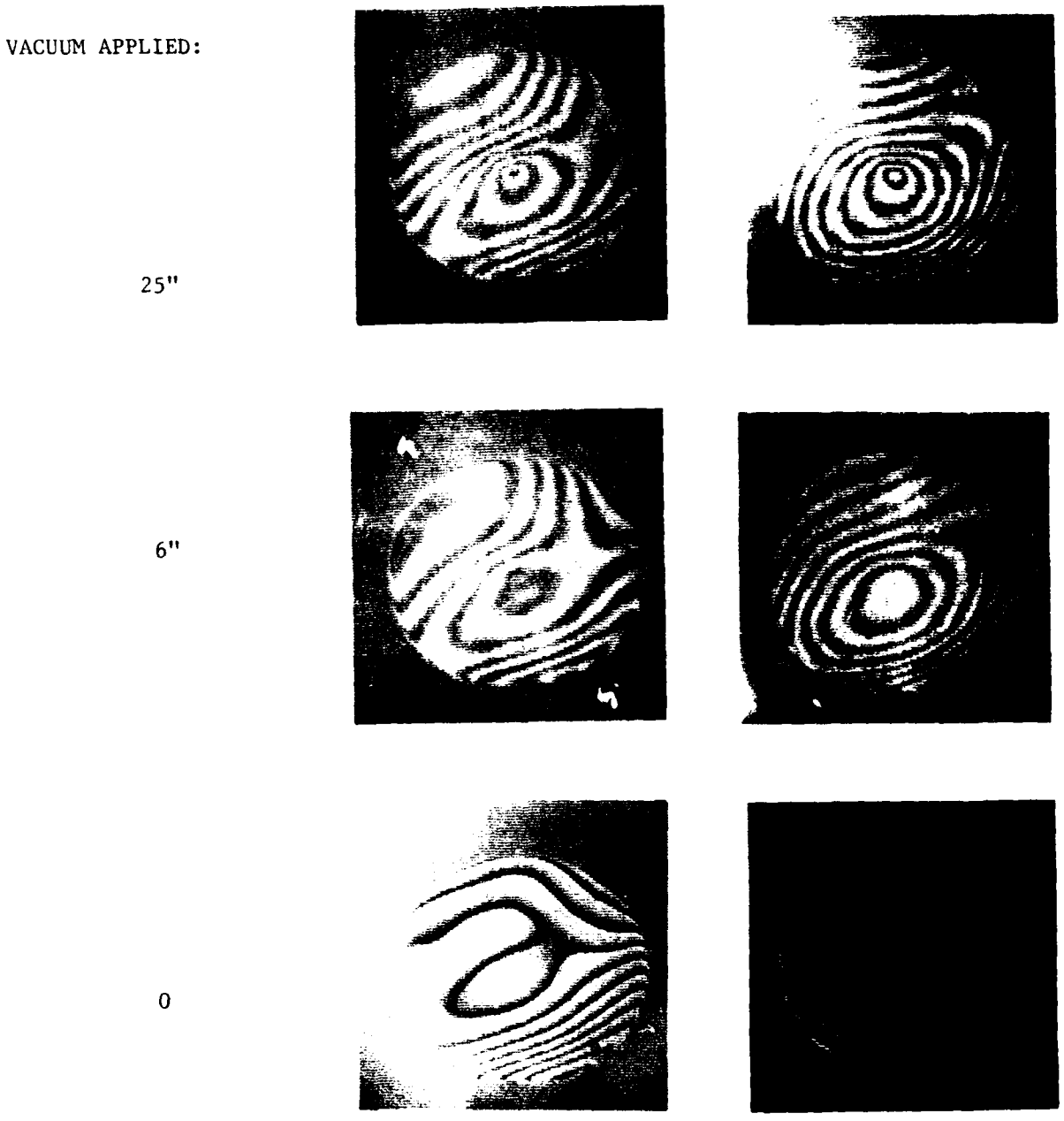


Figure 4.5 Optical Interferograms of Wafer E8 (pCz Medium Oxygen Grade) Before and After the Oxide Was Etched Away, Taken Under Differing Vacuum Conditions.

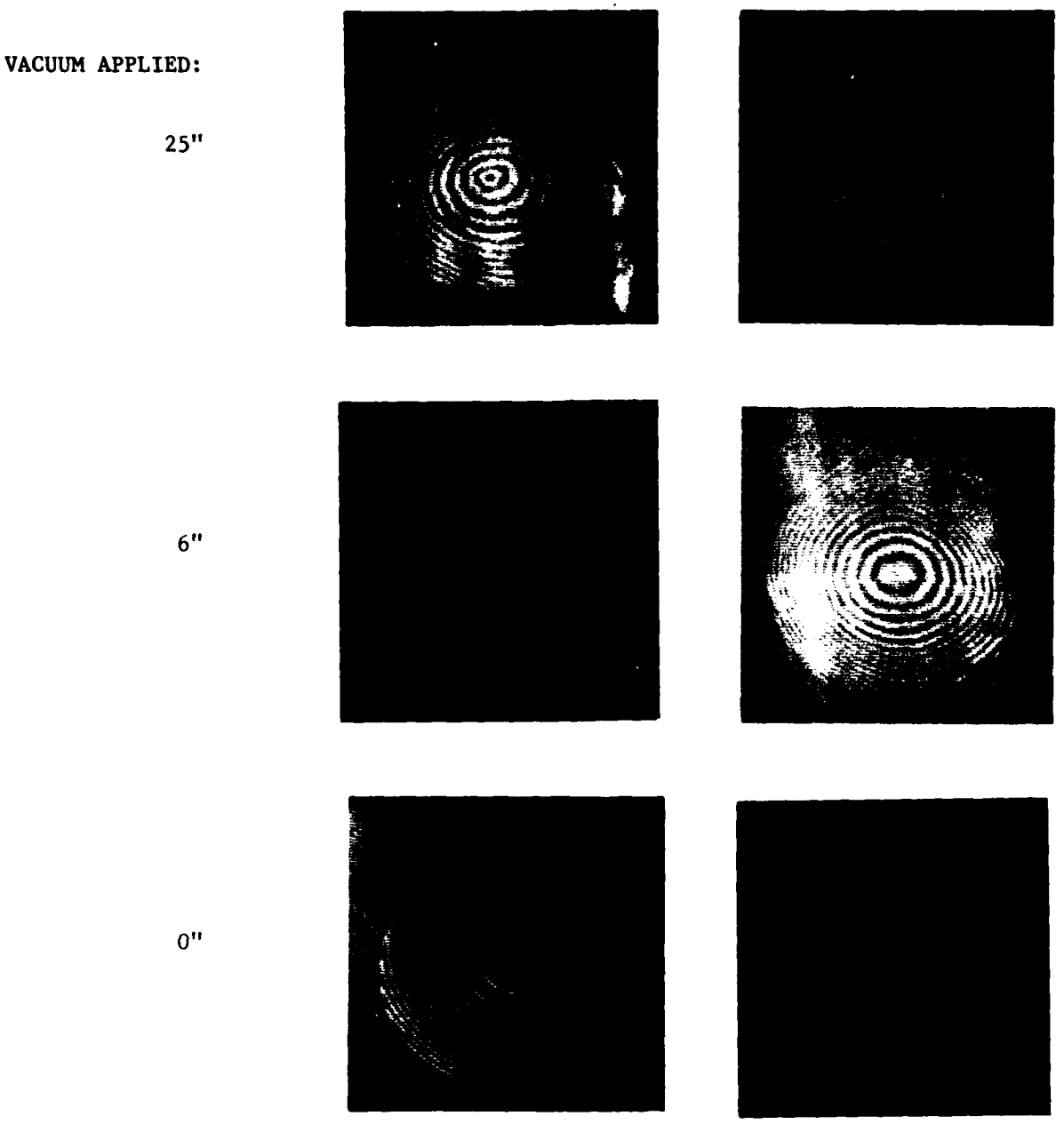
The nCz high oxygen grade wafer results are shown in Figure 4.6. This wafer was strongly dished under all conditions, making accurate fringe counts difficult.

The sensitivity of the Tropel wafer flatness analyzer was reduced until the fringes were clearly visible on the display. This calibration was used for wafers E8 and E12, while wafer E4 was examined with a more sensitive calibration setting.

The interferograms were analyzed quantitatively as follows. The surface deformation was determined by counting fringes. Since the samples are all concave, the surface height increases steadily from center to edge. The depth of the concavity is given by the mean value of the height of the edges. Radius of curvature R is determined by the approximation

$$R = \frac{D^2}{8cF} \qquad (4\text{-}4)$$

where D is the wafer diameter, C is the Tropel calibration factor, and F is the total fringe count from edge to edge [8]. The calibration factors are 0.55 micrometers/fringe for sample E4, and 2.14 micrometers/fringe for samples E8 and E12. The measured fringe counts along two axes, for all vacuum conditions, are shown in Table 4-3. The stress level is computed from expression (4-2), where the term E/6(1-v)) is taken as 3×10^{11} dynes/cm^2 [9]. The oxide thickness t is 34 nm. Substrate thickness T is taken as the average of several measurements at various points spaced around the edge of the wafer. The values were 330μm for E4, 251μm mils for E8, and 254μm for E12. Each wafer was non-uniform in thickness as determined by interferograms taken with the wafer held on a flat vacuum chuck. The taper was between 75 and 100μm for each wafer. The probable cause of the taper was imperfect alignment of the wafer in the mounting fixture used for thinning, due to the precautions taken to protect the oxide surface from damage. Table 4-3 shows the stress level in the oxide computed from expression (4-2), and the maximum stress σ_m in the silicon substrate, computed from expression (4-3).



OXIDE THICKNESS: 34 nm

Figure 4.6 Optical (Interferograms of Wafer E12 (nCz High Oxygen Grade) Before and After the Oxide was Etched Away Taken Under Differing Vacuum Conditions.

The X-ray data are also shown in Table 4-3. The X-ray measurements are very time consuming and only one wafer was characterized. Interestingly, the X-ray data show that the wafer is crystallographically crowned, or convex, as indicated by the negative sign on the radius of curvature. This could happen if the wafer is distorted during polishing. The angular deviation away from perfect (100) surface orientation would be about 0.02 degrees at the edge of the wafer, an amount too small to have any significance in processing. This crystallographic curvature would also help to explain the tendency of all of our wafers to take a concave surface shape, as the crystal lattice curvature is relieved during thermal processing.

The axes for the X-ray scans are only approximately in line with the axes chosen for the optical measurements. The radius of curvature for each axis was taken from a graphical fit of the rotation of the wafer needed to maintain the Bragg condition against wafer translation.

The data in Table 4-3 show that there is generally a lower indicated stress when the vacuum applied to the sample is lower. Apparently, the wafer distortion caused by the applied vacuum interferes with the measurement even in the differential mode. The data taken optically at 0 and 6 inches appled vacuum is generally in good agreement. The stress measured by X-ray is slightly higher than the optical data. This might be due to the choice of different axes for the case of the X-axis, while the discrepancy for the Y-axis between 4.0 for the optical data and 5.0 for the X-ray data may reflect the accuracy limits of both methods. The stress values for wafers E4 and E8 range from 2.3 to 4.0 x 10^9 dyne/cm^2, in agreement with the value 3.0 x 10^9 typically reported in the literature for thermal oxides. Wafers E12 shows a 4.9 x 10^9 stress for the Y-axis. This high value may be an exceptional case due to the high residual stress in this wafer. Characterization of three other nCz high oxygen grade wafers similar to E12 showed one wafer of high surface curvature, and two wafers of lower curvature, as measured interferometrically before processing. Our conclusion is that the available evidence does not show a significant difference in stress levels between the float-zone, medium oxygen grade, and high-oxygen grade Czochralski wafers used for this study.

Table 4-3. Determination of Oxide Stress by Optical and X-Ray Methods

Sample	Axis	Vacuum Applied	Fringe Counts		Radius of Curvature (m)		Oxide Stress Dyne -cm^2	Max. Si Stress Dyne -cm^2
E4	X	25	11.0	19.0	232	135	3.0E9	1.2E6
E4	X	6	6.0	12.0	426	213	2.3E9	9.3E5
E4	X	0	X-Ray Data		-241	2000	4.5E9	1.8E6
E4	Y	25	12.0	24.0	213	107	4.5E9	1.9E6
E4	Y	6	8.0	18.5	320	138	4.0E9	1.6E6
E4	Y	0	X-Ray Data		-121	-326	5.0E9	2.1E6
E8	X	25	5.5	11.0	119	60	4.7E9	2.5E6
E8	X	6	3.0	6.0	219	110	2.5E9	1.4E6
E8	X	0	3.0	6.0	219	110	2.5E9	1.4E6
E8	Y	25	13.0	18.0	51	37	4.2E9	2.3E6
E8	Y	6	9.0	12.5	73	53	3.0E9	1.6E6
E8	Y	0	8.0	11.0	82	60	2.5E9	1.4E6
E12	X	25	22.0	27.0	30	24	4.3E9	2.3E6
E12	X	6	18.5	22.5	36	29	3.5E9	1.9E6
E12	X	0	22.5	26.5	29	25	3.5E9	1.9E6
E12	Y	25	24.0	29.0	27	23	4.3E9	2.3E6
E12	Y	6	24.5	30.0	27	22	4.8E9	2.6E6
E12	Y	0	14.5	20.5	45	32	5.2E9	2.8E6

4.2 RAMP TEST

An extensive series of ramp tests on MOS capacitors of a standard size (1000μm x 1000μm) was performed for each representative wafer, which contains about 40 chips, by using a Keithley automatic test system. The ramp test was made destructively at room temperature on the whole wafer, which was vacuum-mounted on a test chuck. A 40-pin probe card was used to make contact to ten bonding pads of MOS capacitors at a time and to one substrate bonding pad. The voltage ramp used for this test has a voltage range of 0-32 volts with a 0.2 volts increment and a 10 milliseconds dwell time. The polarity of the gate voltage was appropriately chosen to maintain the depletion mode for the MOS capacitors. This polarity choice simulates the normal operation mode of enhancement MOSFETs. On completion of ramping on each chip, the wafer was automatically stepped to a next chip for the subsequent ramping. The breakdown events at each voltage interval were summed over the whole wafer by the DEC PDP-11 computer of the Keithley system. Figures 4.7-4.19 show the histograms of the percentile cumulative device failure (% CDF) vs. electric field. The electric field interval along the x-axis in the figures was obtained by dividing the voltage interval 1.5 volts, which was chosen originally as the summing interval during the histogram construction in the Keithley software, by the oxide thickness. Each histogram corresponds to a single wafer which contains about 40 chips, each chip having ten standard square-shaped (1000μm x 1000μm) MOS capacitors. The breakdown events near the zero field, which are associated with gross oxide defects are of no interest and were excluded by setting a cut-off voltage of two volts in the histogram. Also, events due to open probe contacts, which piled up at the upper end of the ramp voltage range, namely at 32 volts, were excluded from the histogram. Poor probe contacts and zero field breakdown events often reduced the sample size of a single histogram appreciably from the originally available sample size of about 400 capacitors. Each histogram represents a particular wafer lot and substrate type, a particular oxide thickness, a particular substrate type, and a particular ion implant condition.

As seen from the histograms (Figures 4.7-4.19), an appreciable number of breakdown events occur in the intermediate electric field range. This is a characteristic feature common to all dry oxides. It is well known that oxidation in dry O_2/HCl mixture drastically reduces the intermediate range

breakdown. Our gate oxide was deliberately grown in the dry oxygen gas only for the present work to increase the failure at the intermediate electric fields. This will amplify the effect of the substrate on the TDDB and make it easier to detect in the histogram. For this reason and because of a high density of fixed oxide charge in the dry oxide, most of the industry gate oxides are grown with the addition of HCl gas (usually 3-5%). Note that there are two groups of histograms in our results, one with a pronounced bulge at the intermediate electric field (Figures 4.7, 4.9, 4.10, 4.12, 4.13, and 4.18) and the other without any appreciable bulge (Figures 4.8, 4.11, 4.14, 4.15, 4.16, 4.17, 4.19). We believe that the substrate effect on TDDB manifests itself as a bulge, i.e. an increased failure, at the intermediate field (~7MV/cm) shown in the histogram. Table 4-4 shows the summary of Ramp Test results. From these results, three observed facts emerge:

1) All of the MOS capacitor samples fabricated on a Czochralski wafer and having the oxide thickness >30.0nm show a very pronounced bulge in the histogram. See Figures 4.7, 4.9, 4.10, 4.12, and 4.13.

2) All of the samples fabricated on a float zone wafer (low O_2 content) do not show any appreciable bulge. See Figures 4.8, 4.11, 4.14, and 4.17).

3) For samples fabricated on a Czochralski wafer with an oxide thickness <30.0nm, the existence of the bulge is not very clear. See Figures 4.13, 4.15, 4.16, 4.18, and 4.19.

4.3 ACCELERATED LIFE TEST

Accelerated life tests were performed on a limited number of MOS capacitors on selected chips in order to provide a reference from which a use life of our devices could be predicted. Only very limited data were obtained due to time limitations.

Approximately 40 chips were bonded and packaged in 40-pin DIP packages without hermetic seal for the accelerated life test. The bonded devices in each chip were ten MOS capacitors of a standard size (1000μm x 1000μm) and

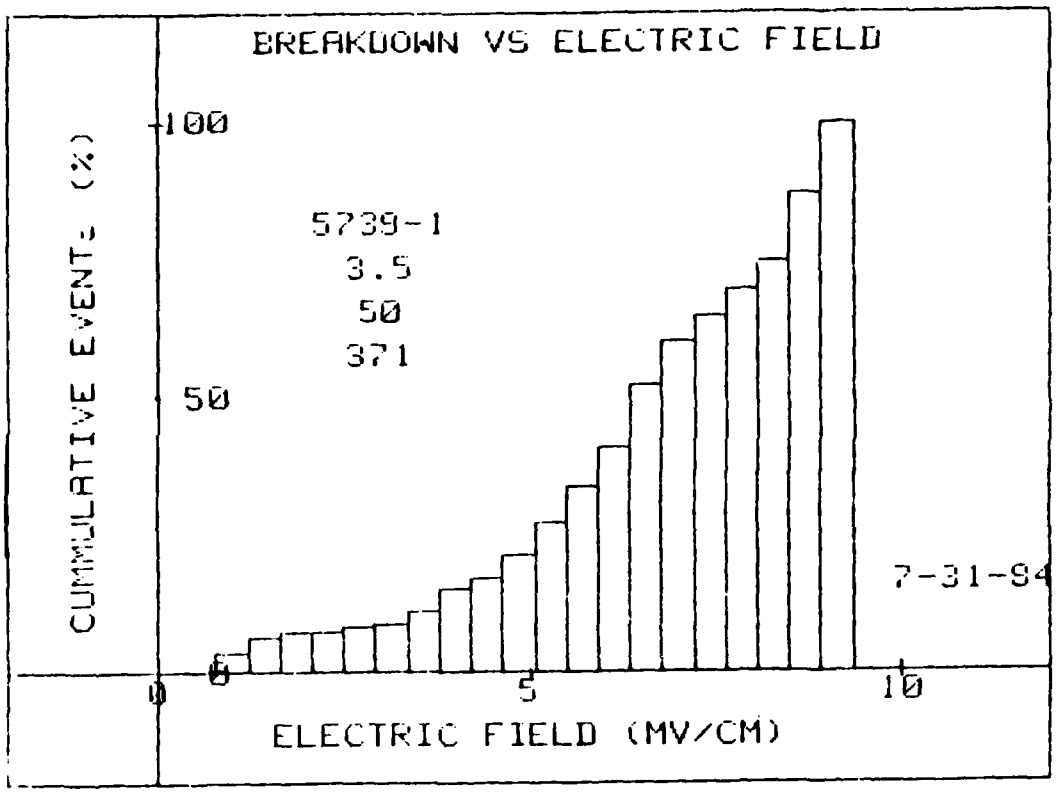


Figure 4.7 Breakdown Histogram (Substrate: Czochralski N-Type, t_{ox} = 35.0nm Sample Size = 371)

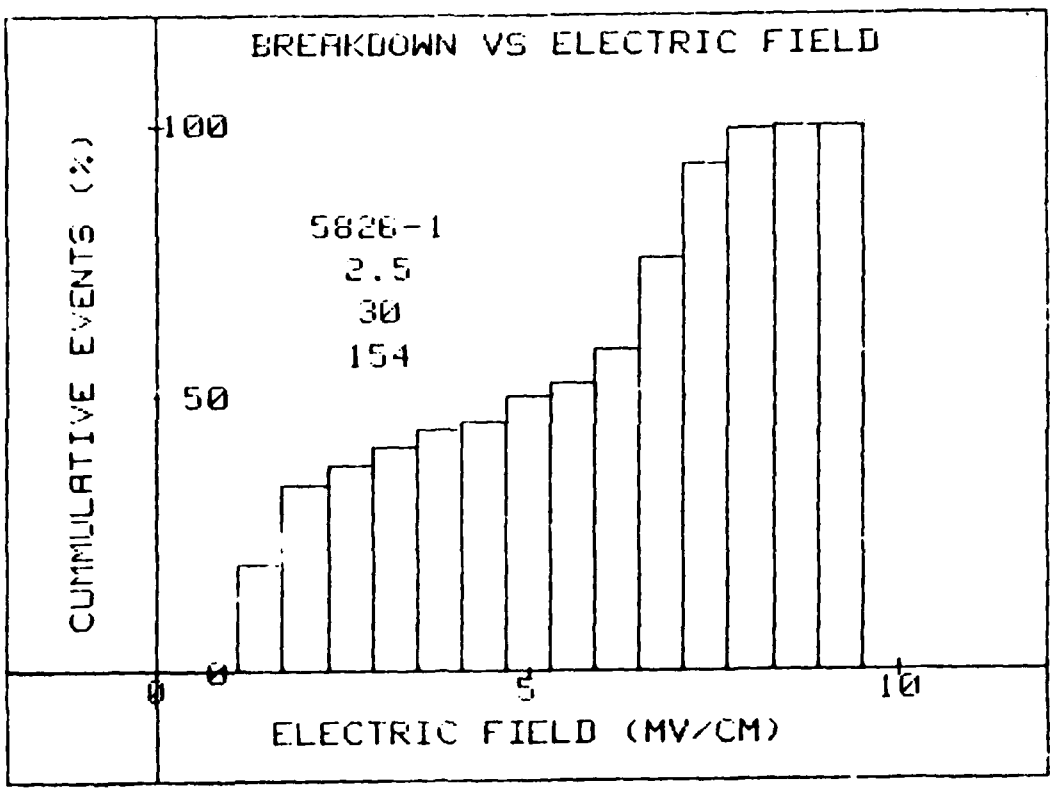


Figure 4.8 Breakdown Histogram
(Substrate: Float Zone N-Type, t_{ox} = 25.0nm Sample Size = 154)

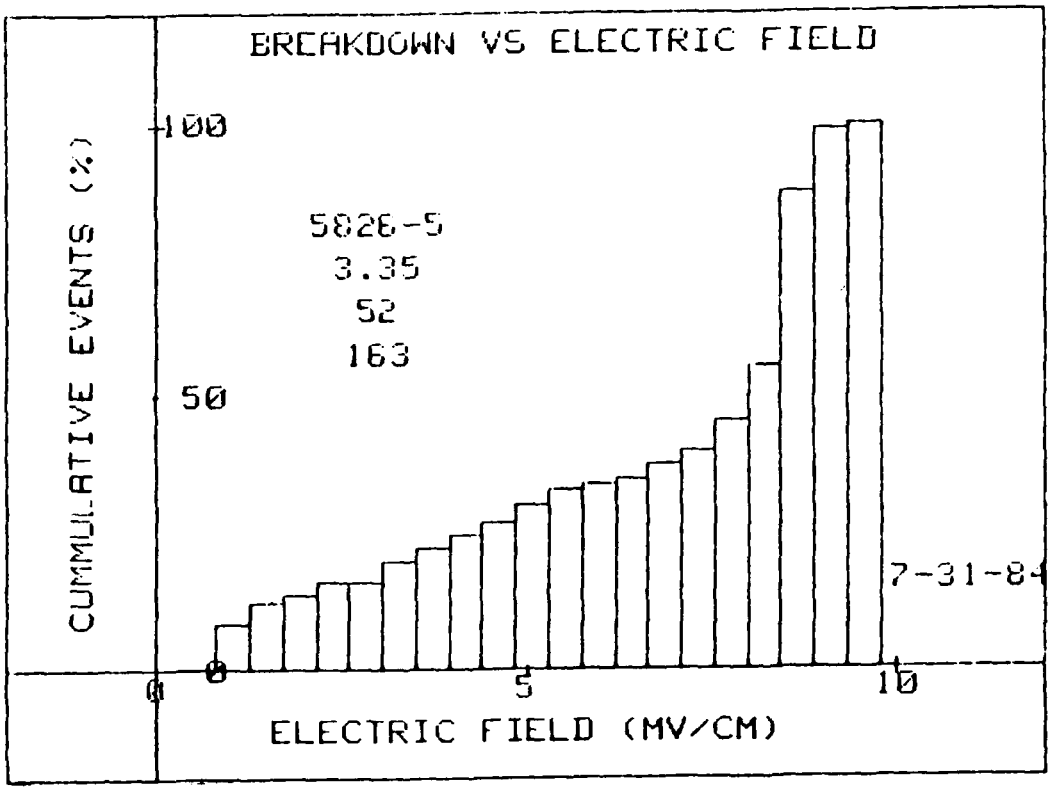


Figure 4.9 Breakdown Histogram
(Substrate: Czochralski P-Type, t_{ox} = 33.5nm Sample Size = 163)

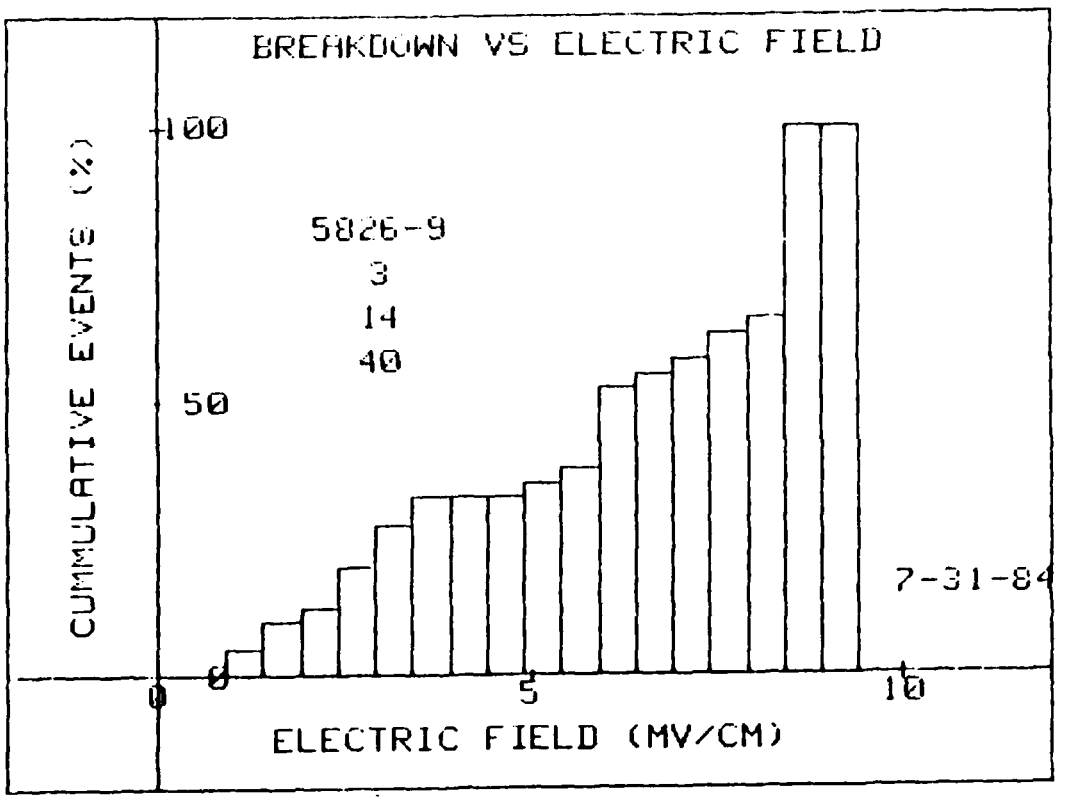


Figure 4.10 Breakdown Histogram
(Substrate: Czochralski N-Type, t_{ox} = 30.0nm Sample Size = 40)

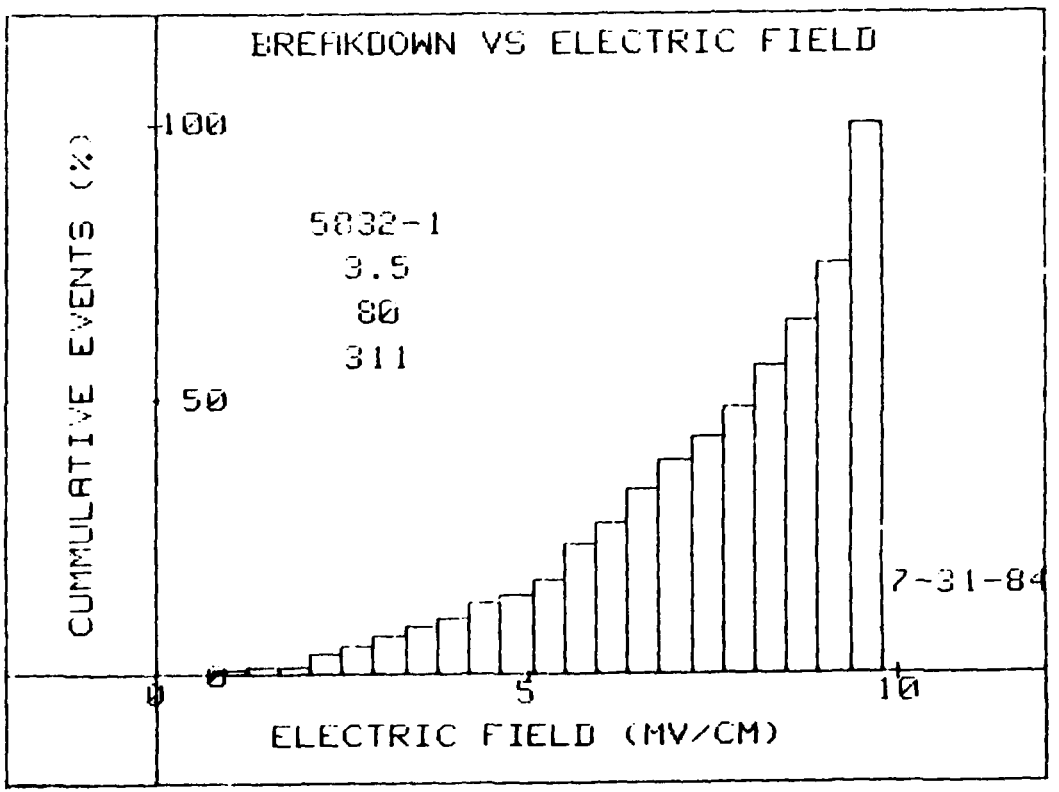


Figure 4.11 Breakdown Histogram
(Substrate: Float Zone N-Type, t_{ox} = 35.0nm Sample Size = 311)

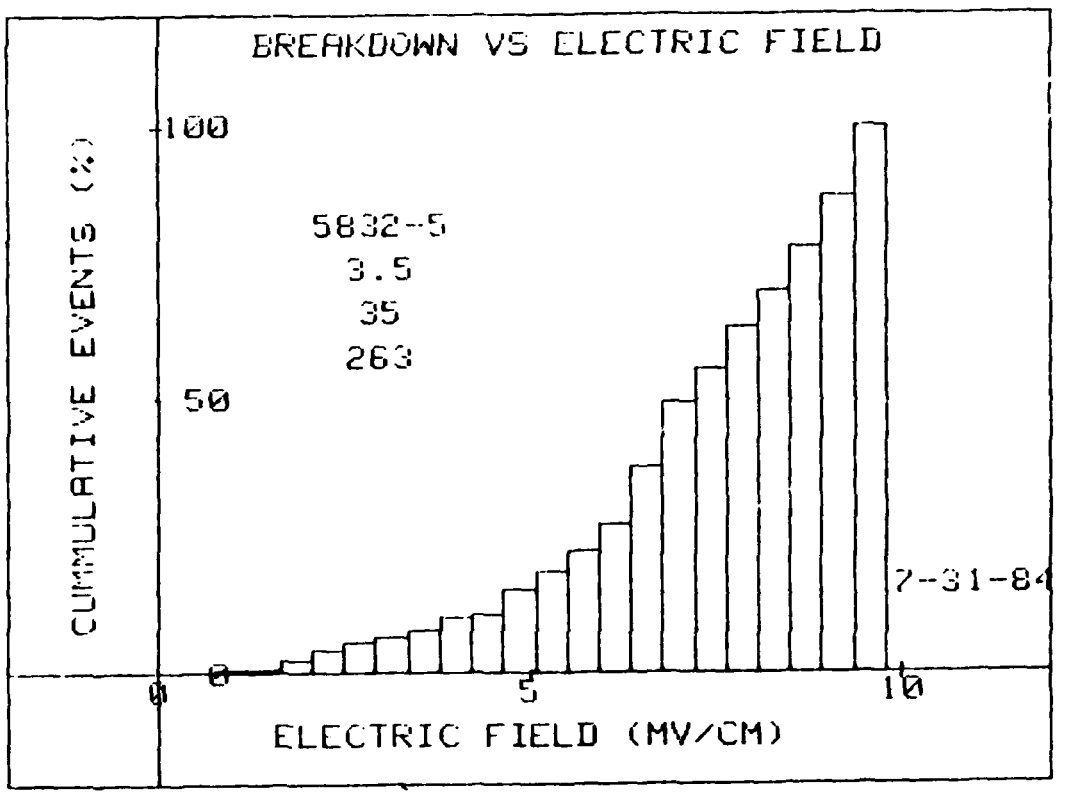


Figure 4.12 Breakdown Histogram

(Substrate: Czochralski N-Type, t_{ox} = 35.0nm Sample Size = 263)

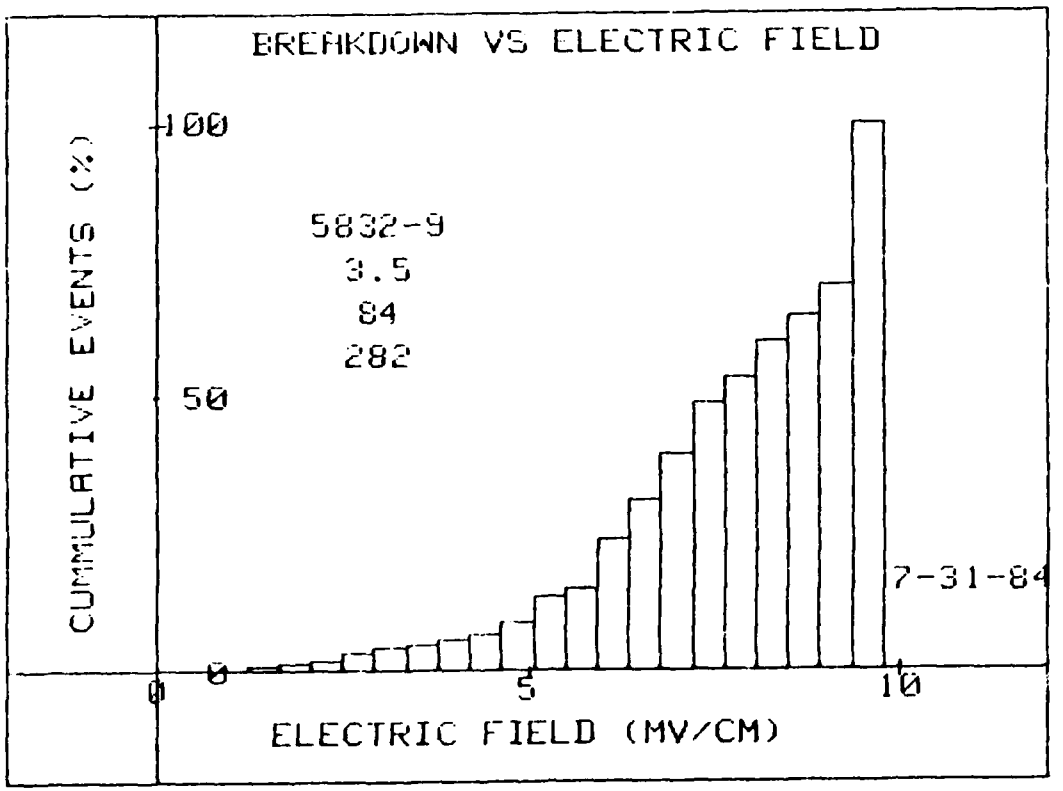


Figure 4.13 Breakdown Histogram
(Substrate: Czochralski P-Type, t_{ox} = 35.0nm Sample Size = 282)

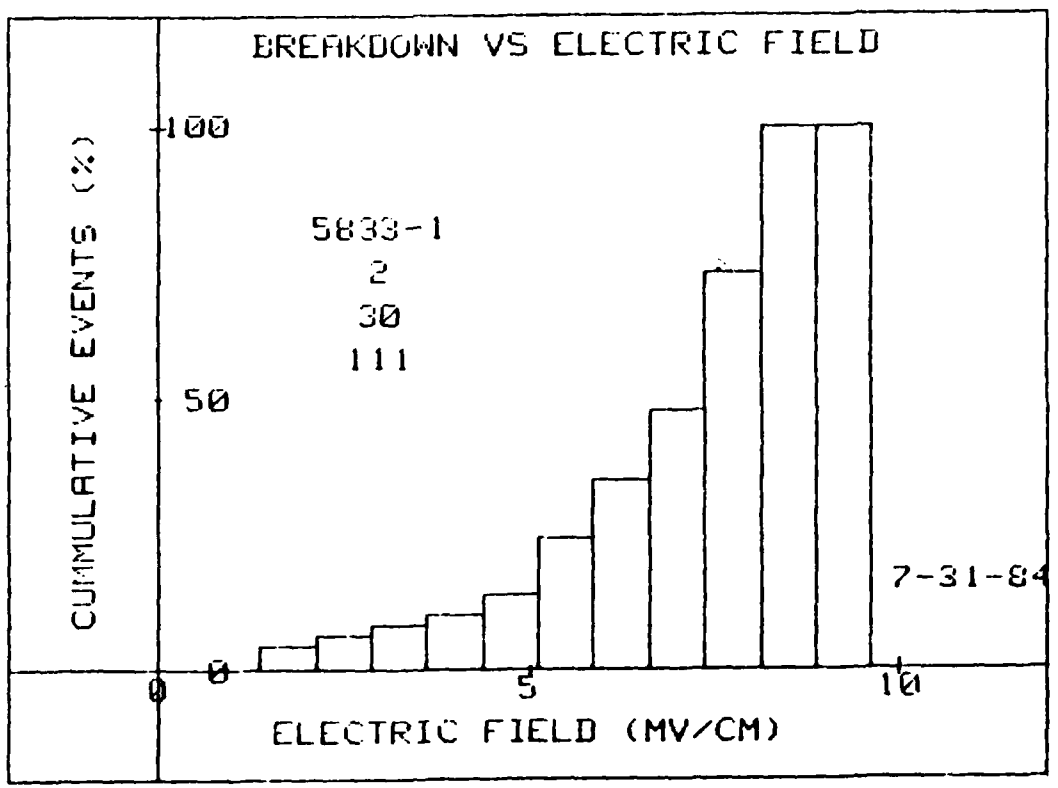


Figure 4.14 Breakdown Histogram

(Substrate: Float Zone N-Type, t_{ox} = 20.0nm Sample Size = 111)

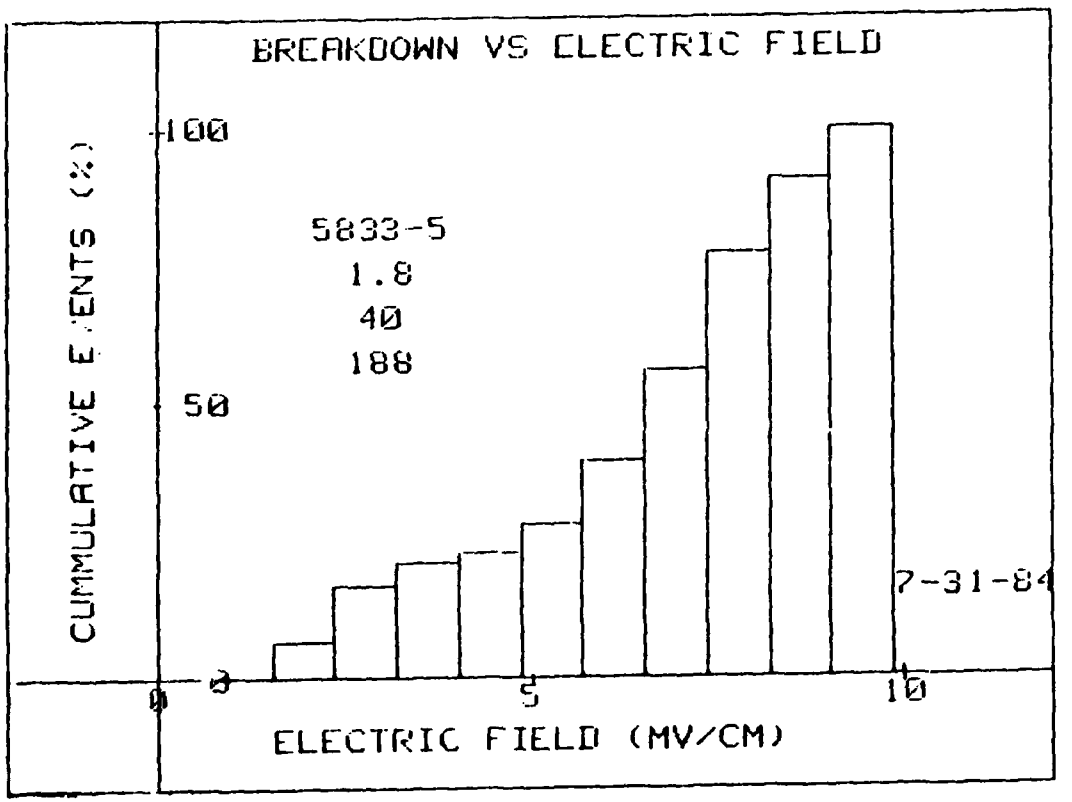


Figure 4.15 Breakdown Histogram

(Substrate: Czochralski N-Type, t_{ox} = 18.0nm Sample Size = 188)

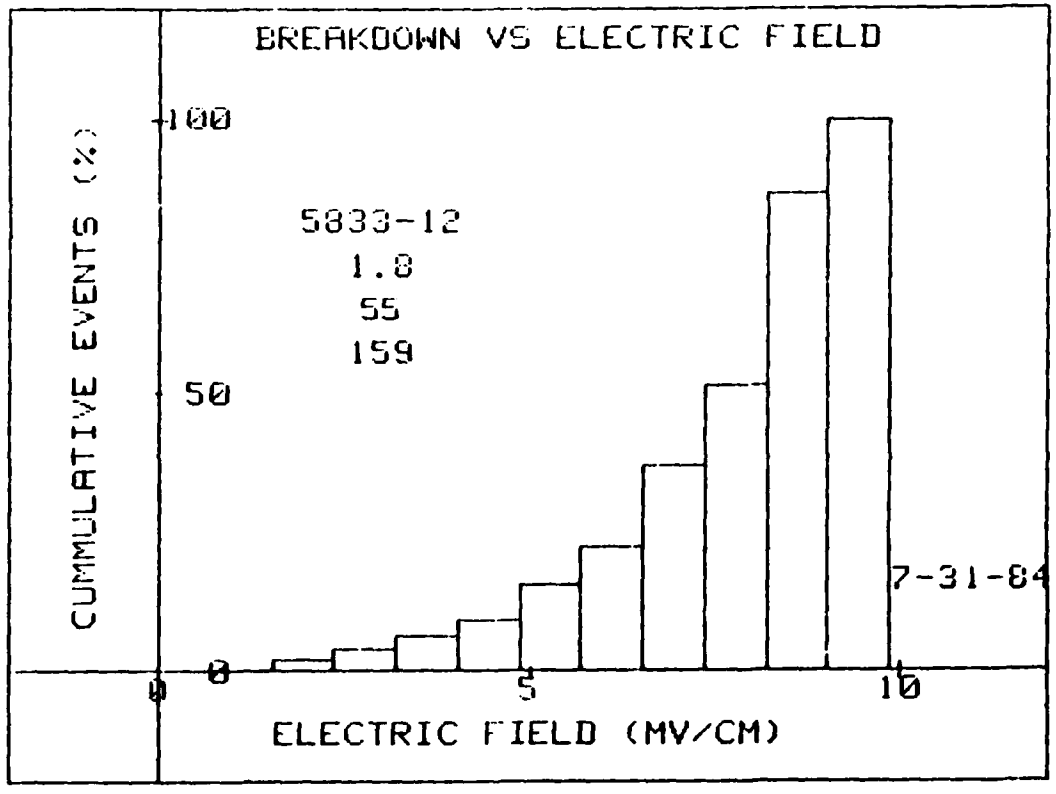


Figure 4.16 Breakdown Histogram
(Substrate: Czochralski P-Type, t_{ox} = 18.0nm Sample Size = 159)

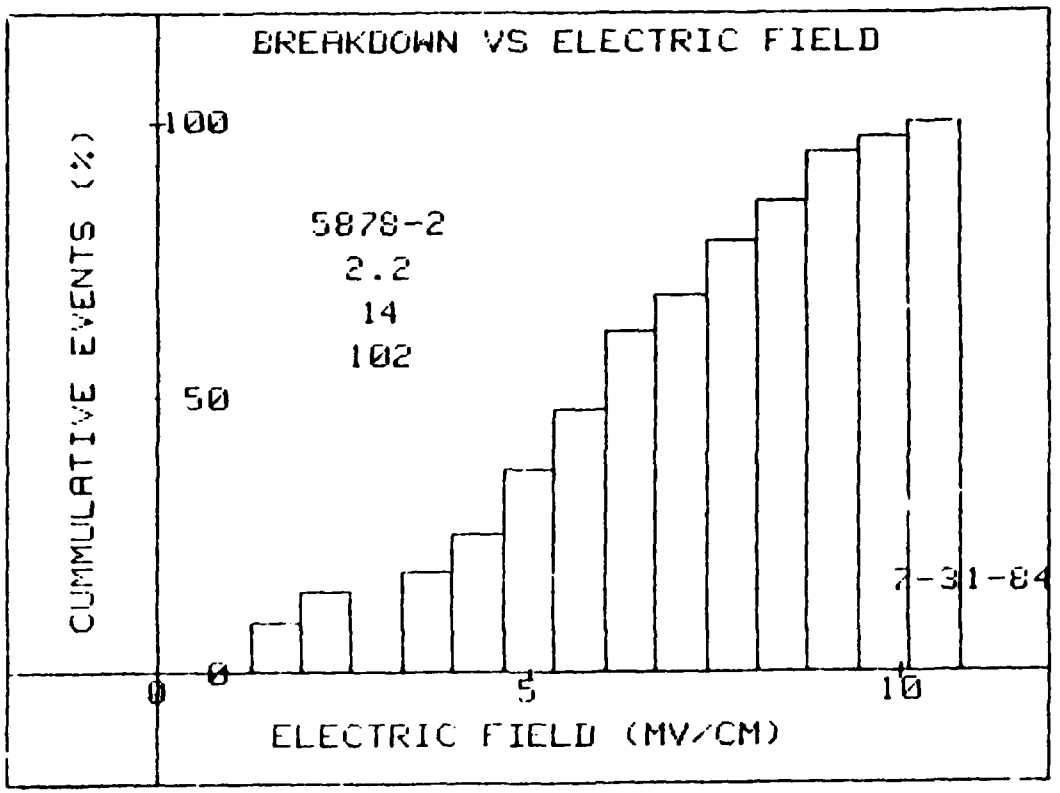


Figure 4.17 Breakdown Histogram
(Substrate: Float Zone N-Type, t_{ox} = 22.0nm Sample Size = 102)

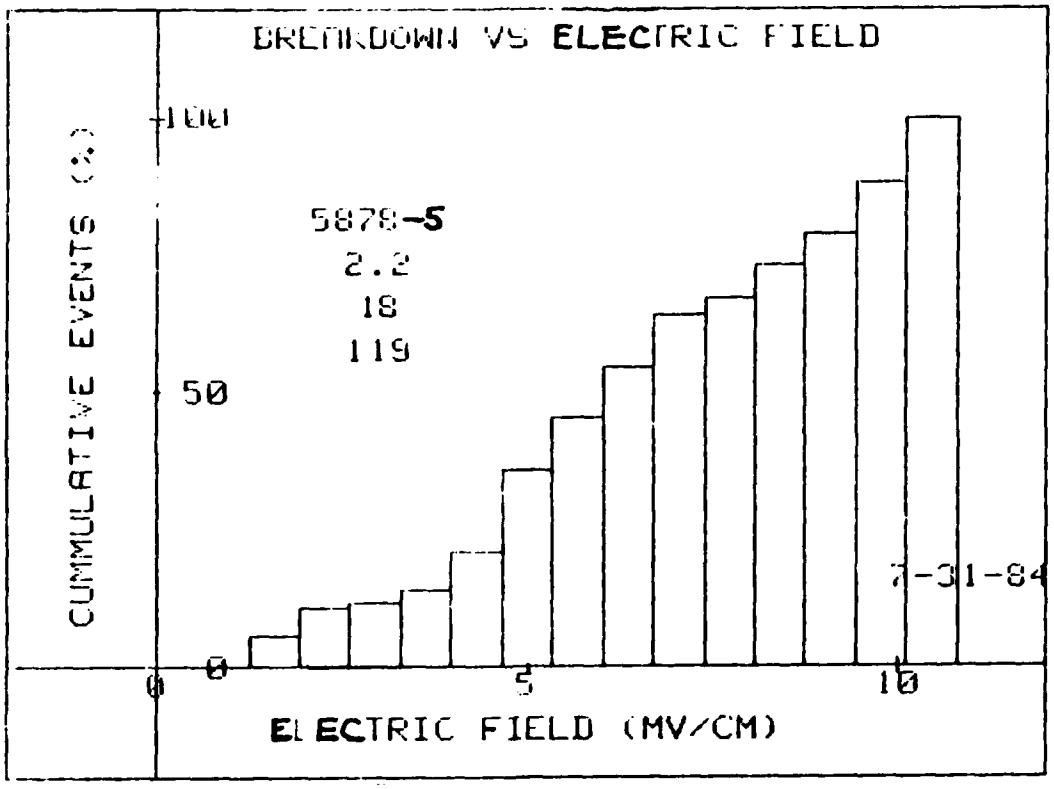


Figure 4.18 Breakdown Histogram

(Substrate: Czochralski N-Type, t_{ox} = 22.0nm Sample Size = 119)

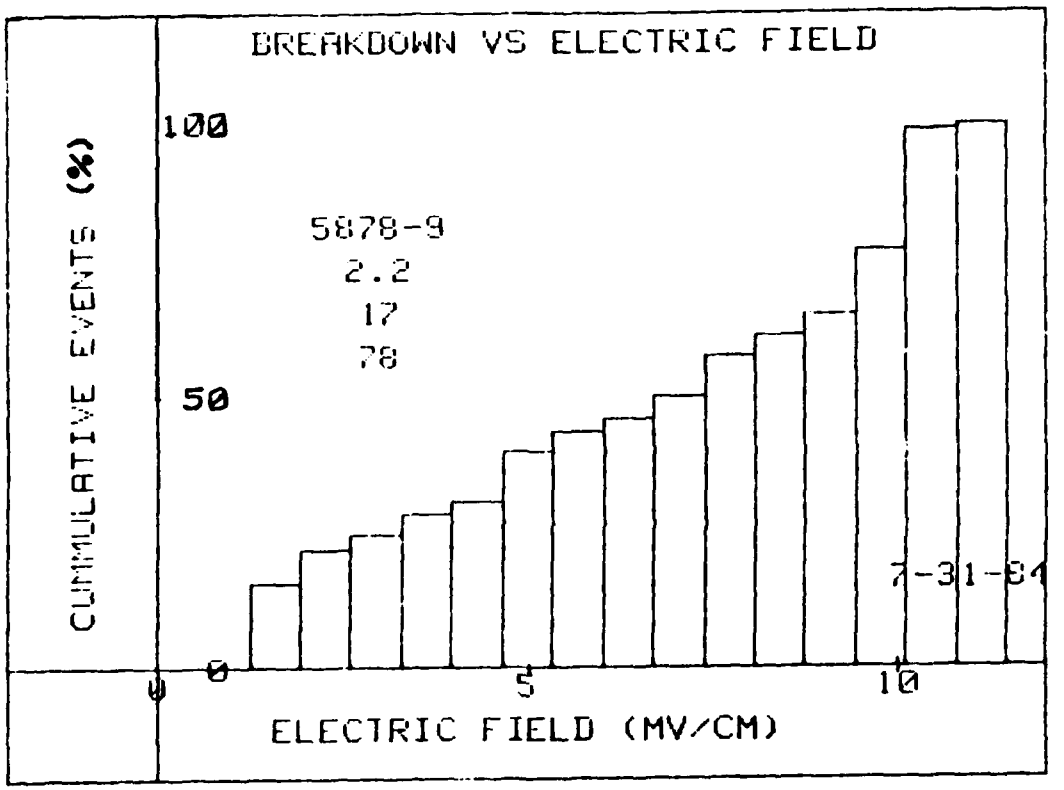


Figure 4.19 Breakdown Histogram
(Substrate: Czochralski P-Type, t_{ox} = 22.0nm Sample Size = 78)

Table 4-4. Summary of Ramp Test Results

Wafer #	Substrate Type	Oxide Thickness (nm)	Total Number of Capacitors Used in the Histogram	Enhanced Failure	Histogram	Implant Polarity of Substrate Under the Gate
5739-1	CZ-N	35.0	371	Yes	Fig 4.7	N
5826-1	FZ-N	25.0	154	-	Fig 4.8	P
5826-5	CZ-P	33.5	163	Yes	Fig 4.9	P
5826-9	CZ-N	30.0	40	-	Fig 4.10	P
5832-1	FZ-N	35.0	311	No	Fig 4.11	N
5832-5	CZ-N	35.0	263	Yes	Fig 4.12	N
5832-9	CZ-P	35.0	282	Yes	Fig 4.13	N
5833-1	FZ-N	20.0	111	No	Fig 4.14	P
5833-5	CZ-N	18.0	188	No	Fig 4.15	P
5833-12	CZ-P	18.0	159	No	Fig 4.16	P
5878-2	FZ-N	22.0	102	No	Fig 4.17	N
5878-5	CZ-N	22.0	119	Yes	Fig 4.18	N
5878-9	CZ-P	22.0	78	-	Fig 4.19	N

four MOSFETs in the same chip were sacrificed because of time limitation during the data acquisition, and vice versa. The temperature chamber used accommodated a maximum of 10 chips at a time and provided temperatures up to 200°C. Connection was made to the devices under test in the chambers through high temperature 44-pin card edge connectors. Each load board card accommodated a single packaged chip. Each MOS capacitor was connected in series with a 2 kilo-ohm resistor on the printed card for the current limiting purposes. A precision D.C. power supply (PD Model 2005) was used to provide a stress voltage to the devices under test. A common 200 ohm load resistor was connected in series between the power supply and all the ten MOS capacitors in each chip to monitor the breakdown events. (See Figure 4.20 for the device connection schematics). A strip chart recorder was used to record the voltage drop across the load resistor. The intent was that each dielectric breakdown event for any of the capacitors under test would cause a current flow through the load loop, thus giving rise to a finite voltage drop across the load resistor. It was discovered that the dielectrically failed MOS capacitor was not a complete short nor had the same resistance for all the failed capacitors. The resistance ranged from almost zero to many megohms, which was in sharp contrast to our previous experience that all of the dielectrically failed capacitors were short-circuited when the devices were hand-probed. For this reason, the monitoring technique did not yield the desired results. The self-healing phenomenon, i.e., becoming open circuited after being dielectrically failed, is not believed to occur easily for the polysilicon gate electrode but is very common to metal electrode such as aluminum.

Because of the failure of our planned automatic monitoring technique, probably due to the current limiting resistors, the failure events had to be monitored by hand intermittently. For each round of monitoring, the bias stress voltage had to be removed and the failed devices were marked off by measuring the resistance of the capacitor with a multimeter (Fluke Model 8020B). This hand monitoring severely limited the sample size and data acquisition capability.

Only one meaningful run was made at 175°C and at bias electric field of approximately 5Mv/cm for eight chips. The initial sample size of 90 capacitors having an oxide thickness of 200°A were screened out at room temperature by applying a stress voltage of 10 volts for 30 seconds. The

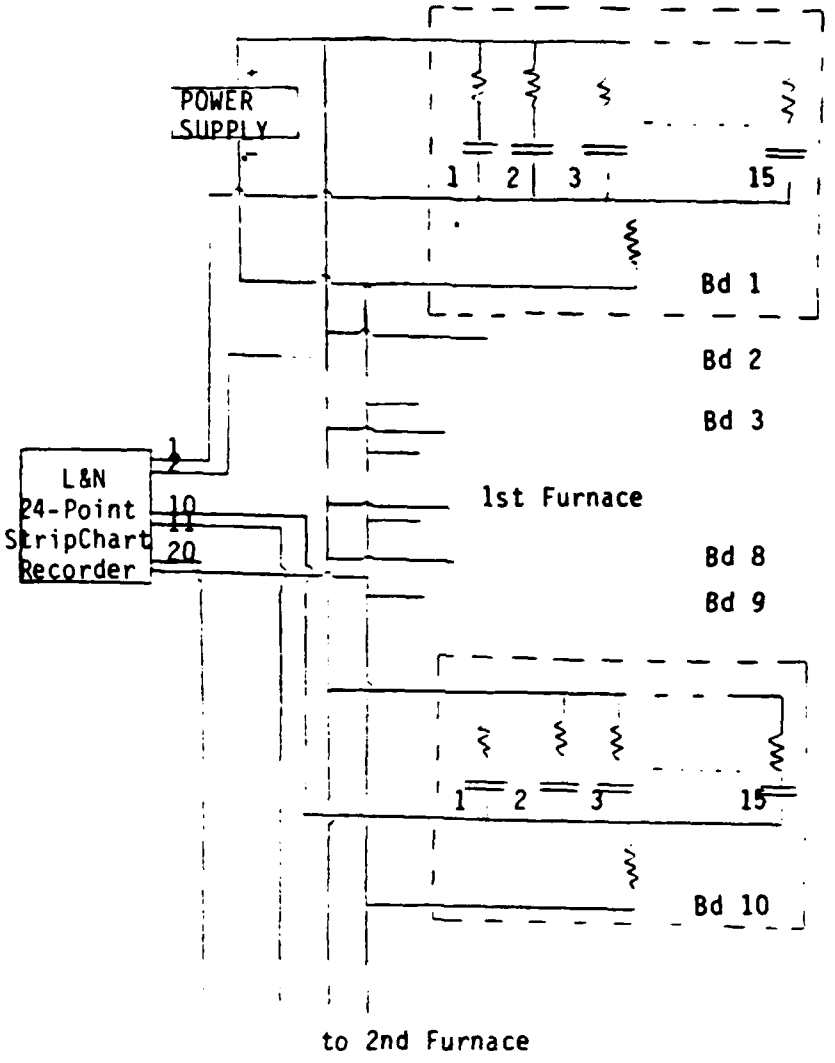


Figure 4.20 Diagram of Accelerated Failure Test Circuit for MOS Capacitors.

survived samples (about 40 capacitors) were loaded in the oven and the oven temperature was raised to 175C in approximately 30 minutes. Immediately a second screening was made at 175C with a zero bias voltage on the survivors. The time at the onset of this second screening was taken as time zero of the accelerated life test. Figures 4.21-4.27 show data for each individual chip. The average time for each monitoring by hand was about one minutes, hence the early data involves a large uncertainty in time axis. The combined data for all chips are shown in Figure 4.28.

Several more runs at different temperatures (150°C and 200°C) and at different bias fields (4Mv/cm and 6Mv/cm) would be needed to provide both the temperature acceleration factor and the field acceleration factor, but, because of time limitation as mentioned earlier, were not possible in this contract. In the meantime, the single data set obtained can be used as a valuable reference point in the use life projection of devices fabricated in this program, if appropriate acceleration factors in the literature are used.

4.4 C-V and I-V Measurements

For each representative chip, a C-V measurement at 10KHz was measured on the HP test system primarily for rechecking the gate oxide thickness. Figure 4.29 shows a typical result. The C-V measurement provides the value for the gate oxide thickness (from the maximum saturation capacitance in the accumulation region) which agrees with the value obtained by ellipsometry within 10%.

It also provides the oxide charge density (from the flatband shift), and the total interface state density (from the non-parallel portion of the curve shift). The typical oxide charge density was about $1x10^{11}/cm^2$ but its variation from one wafer to another was not examined.

The DC I-V characteristics were measured by using HP TEACAP test system (HP 9826 computer, HP 4140B PA Meter/DC voltage source, HP 3497A Data Acquisition/Control Unit, HP 492A LF Impedance Analyzer). A linear ramp voltage was applied across the MOS capacitors and the current through the gate oxide was measured as a function of the instantaneous gate voltage at a sweep rate of 1 V/sec. Figure 4.30 shows a typical result. Note that there are a

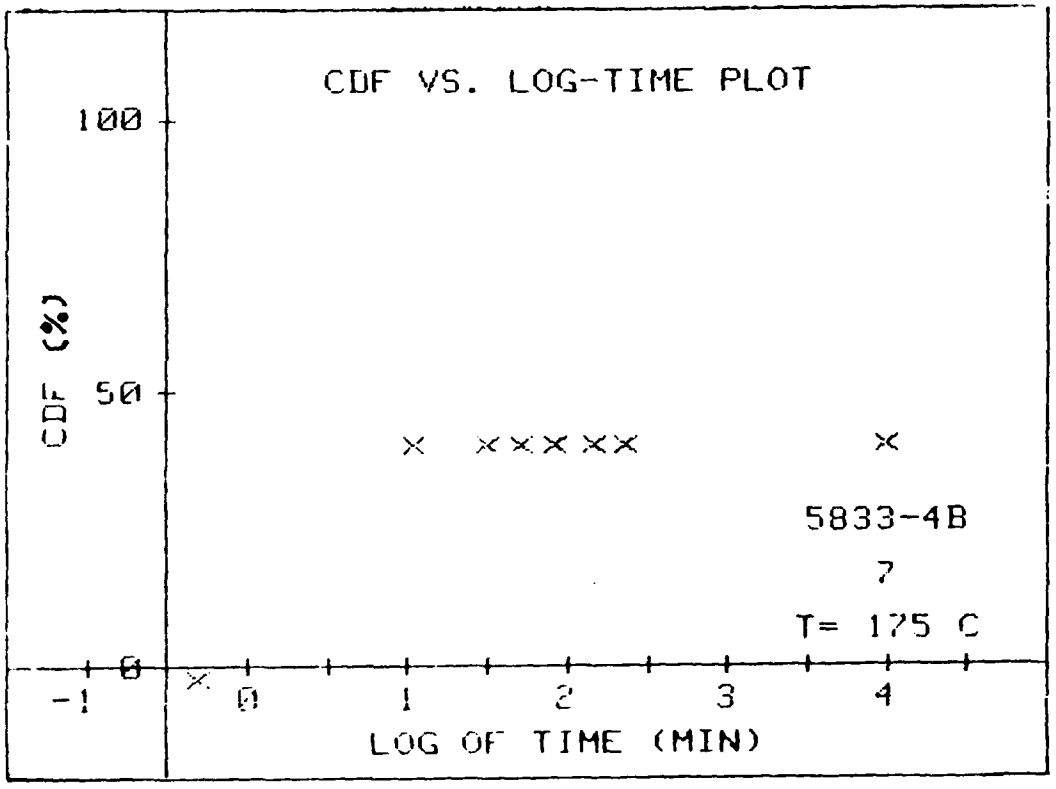


Figure 4.21 Cumulative Breakdown Events vs Time Curve for MOS Capacitors (Substrate: Float Zone N-Type, t_{ox} = 18.0nm T = 175°C) E = 5.6MV/cm, Sample Size = 7

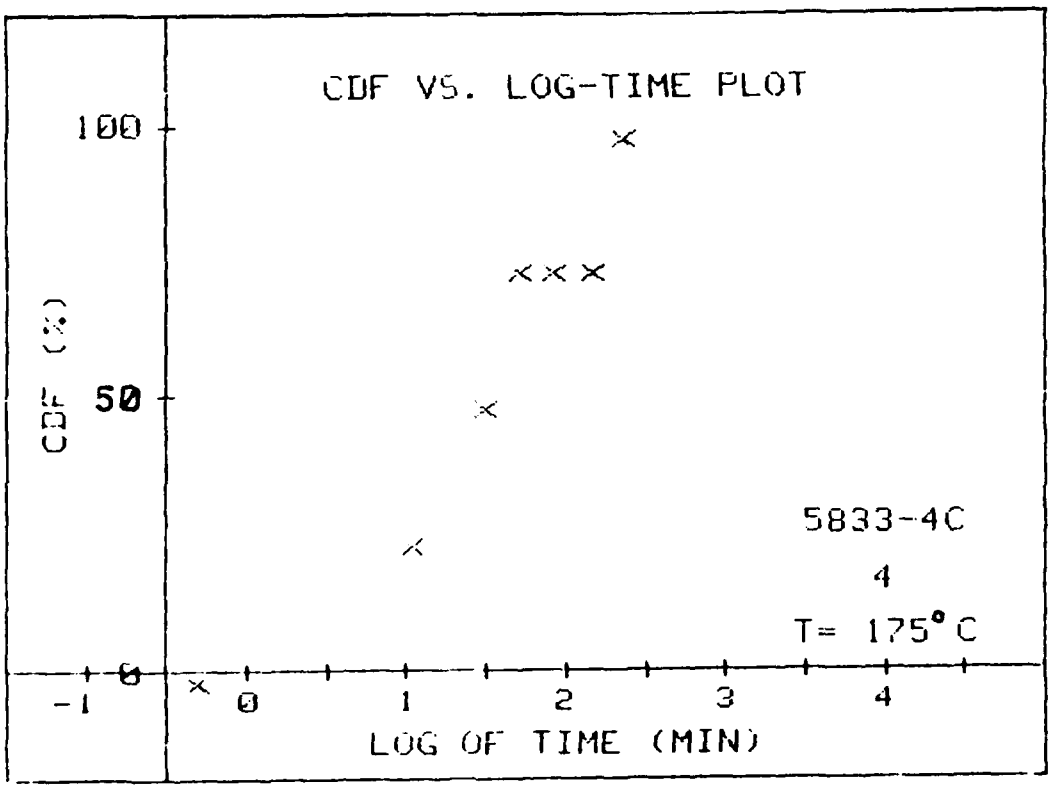


Figure 4.22 Cumulative Breakdown Events vs Time Curve for MOS Capacitors (Substrate: Float Zone N-Type, t_{ox} = 18.0nm T = 175°C) E = 5.6MV/cm, Sample Size = 4

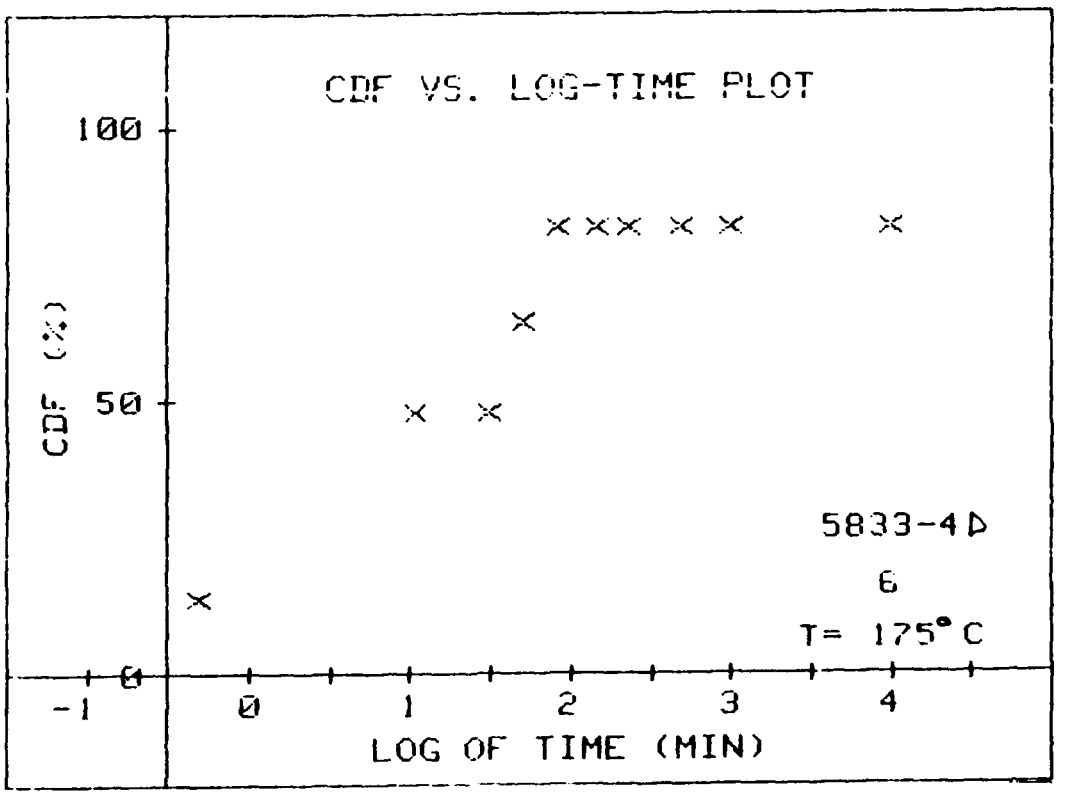


Figure 4.23 Cumulative Breakdown Events vs Time Curve for MOS Capacitors (Substrate: Float Zone N-Type, t_{ox} = 18.0nm T = 175°C) E = 5.6MV/cm, Sample Size = 6

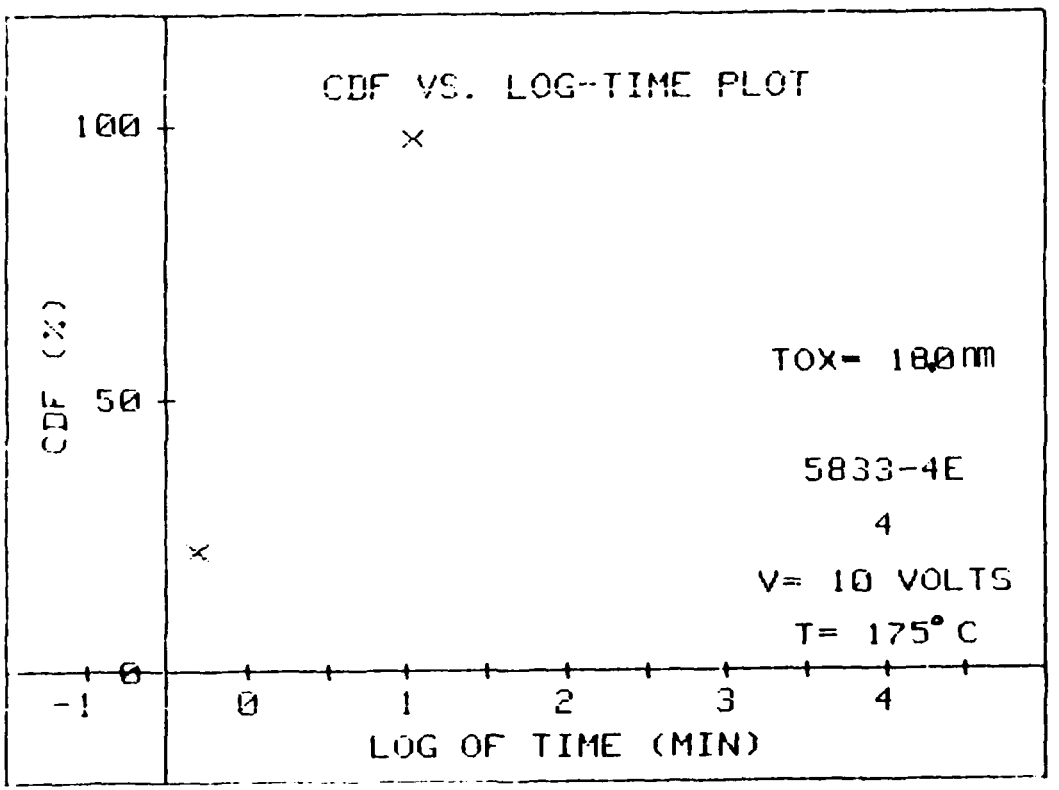


Figure 4.24 Cumulative Breakdown Events vs Time Curve for MOS Capacitors (Substrate: Float Zone N-Type, t_{ox} = 18.0nm T = 175°C, E = 5.6MV/cm, Sample Size = 4)

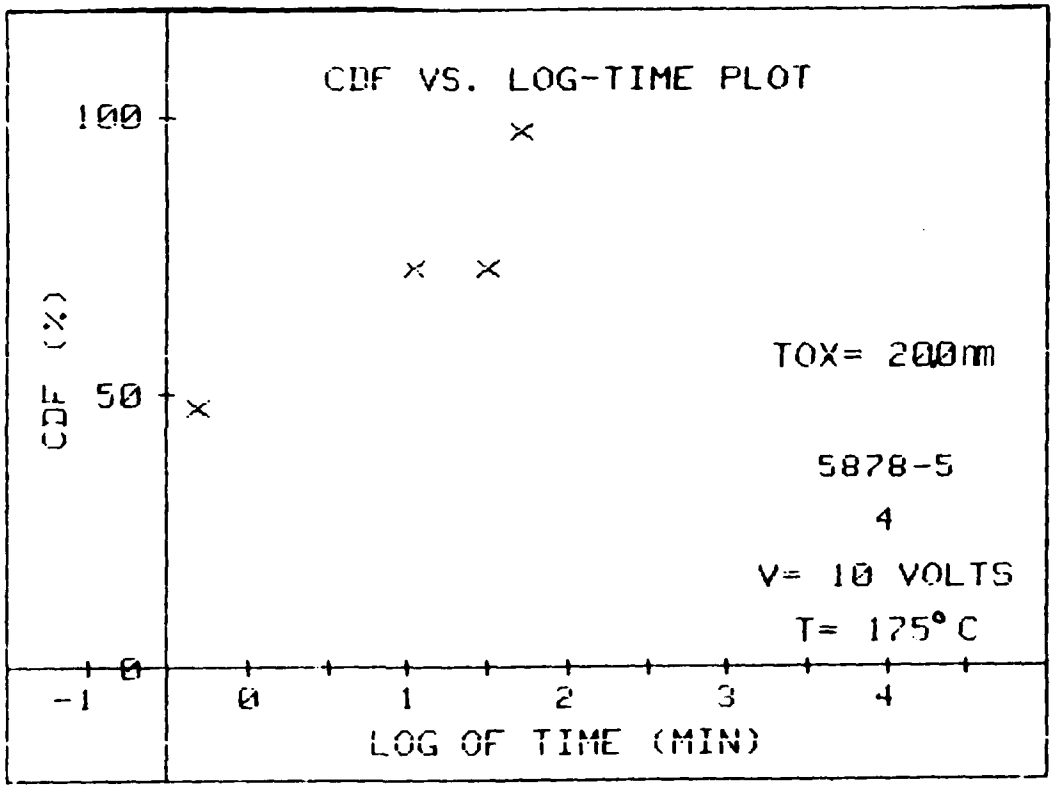


Figure 4-25 Cumulative Breakdown Events vs Time Curve for MOS Capacitors (Substrate: Czochralski N-Type, t_{ox} = 20.0nm T = 175°C, E = 5MV/cm, Sample Size = 4)

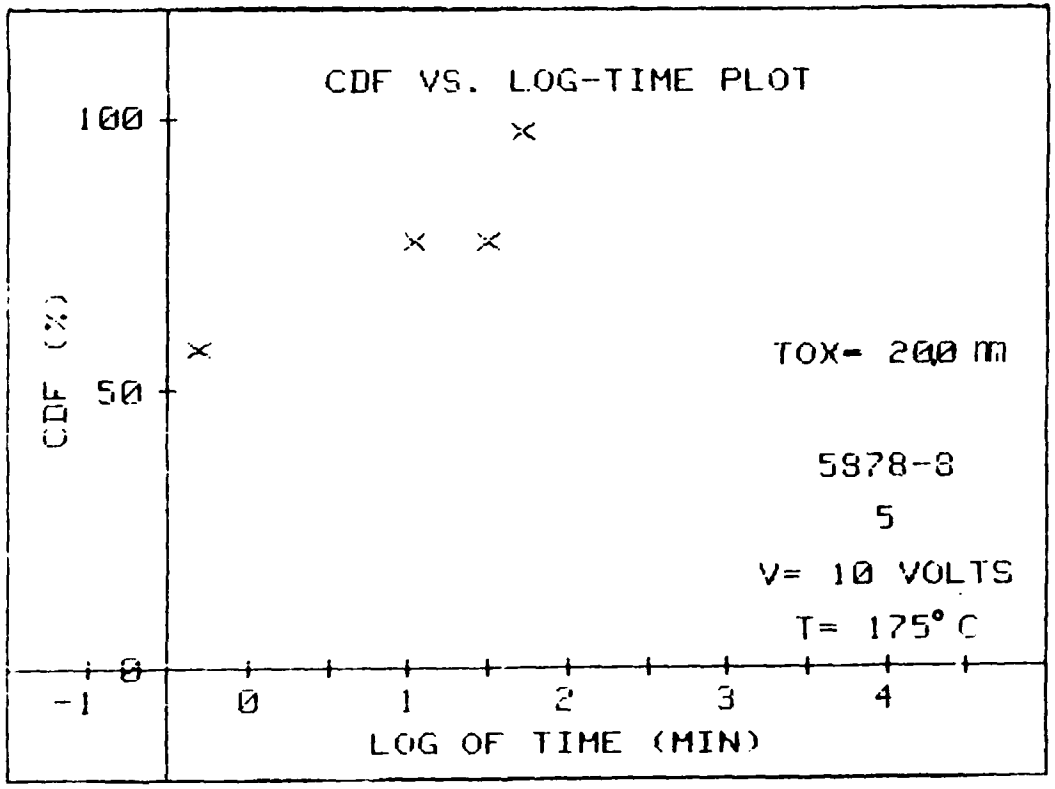


Figure 4.26 Cumulative Breakdown Events vs Time Curve for MOS Capacitors (Substrate: Czochralski N-Type, t_{ox} = 20.0nm T = 175°C, E = 5MV/cm, Sample Size = 4)

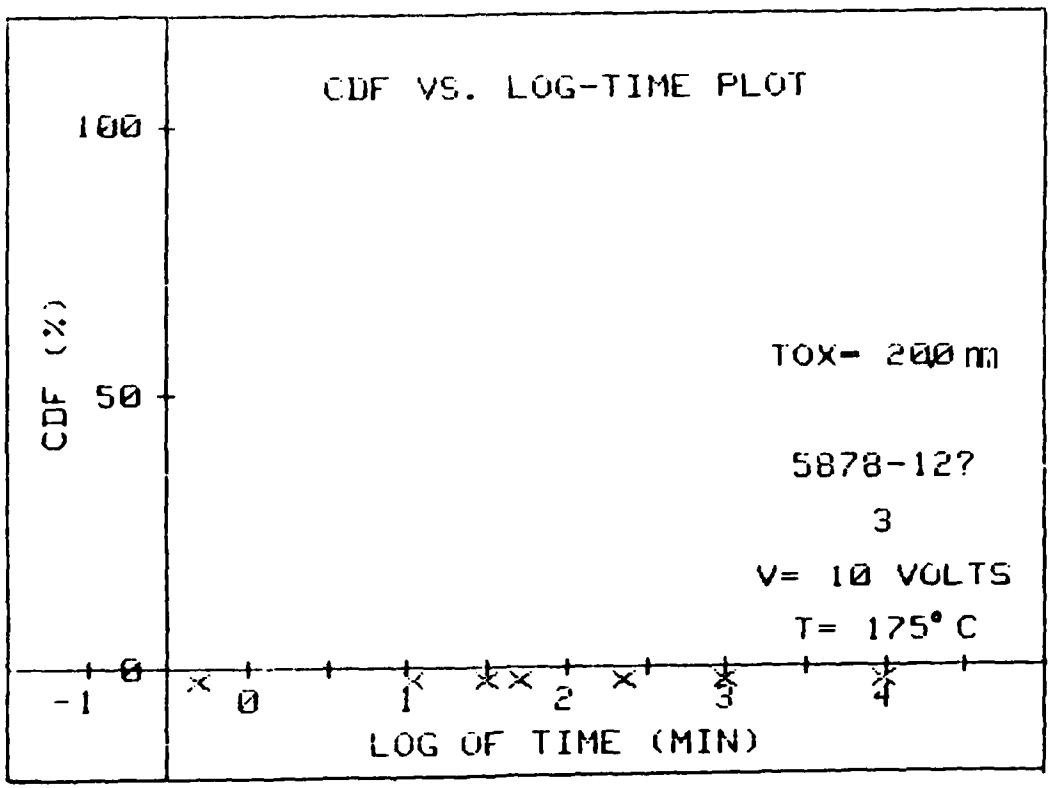


Figure 4.27 Cumulative Breakdown Events vs Time Curve for MOS Capacitors (Substrate: Czochralski N-Type, t_{ox} = 20.0nm T = 175°C, E = 5MV/cm, Sample Size = 3)

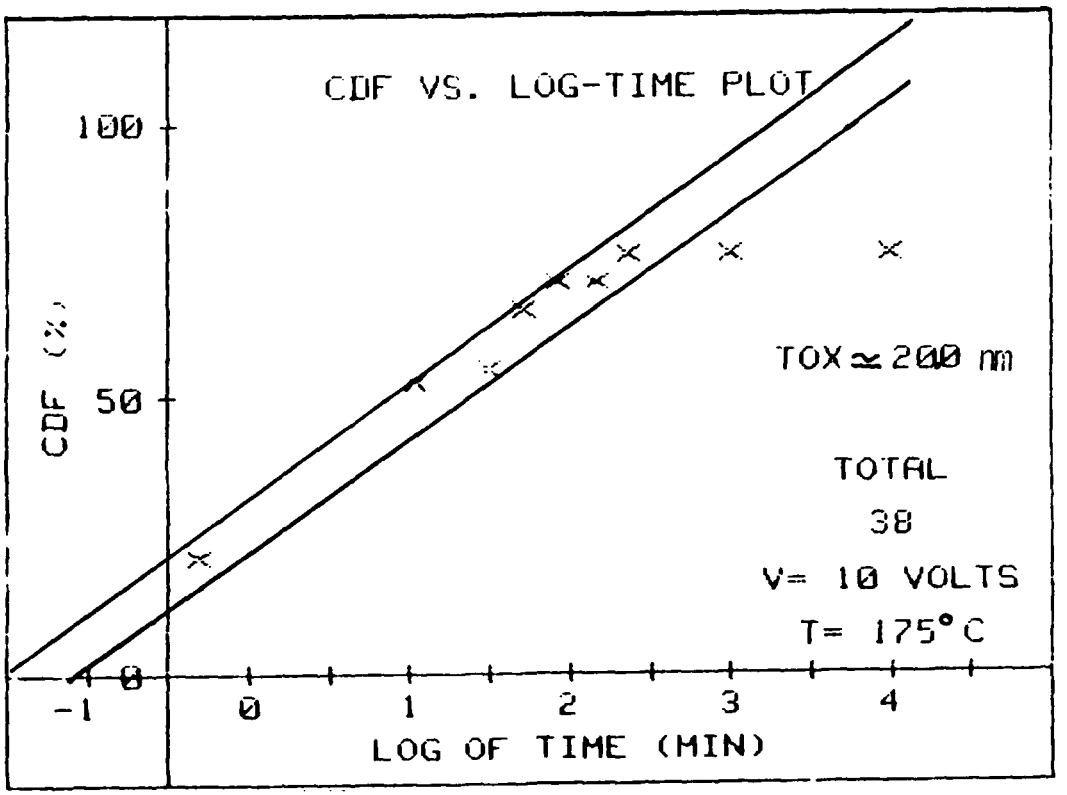


Figure 4.28 Cumulative Breakdown Events vs Time Curve for MOS Capacitors (Substrate: Czochralski N-Type, $t_{ox} \simeq 20.0$nm T = 175°C, E ≃ 5MV/cm, Sample Size = 48)

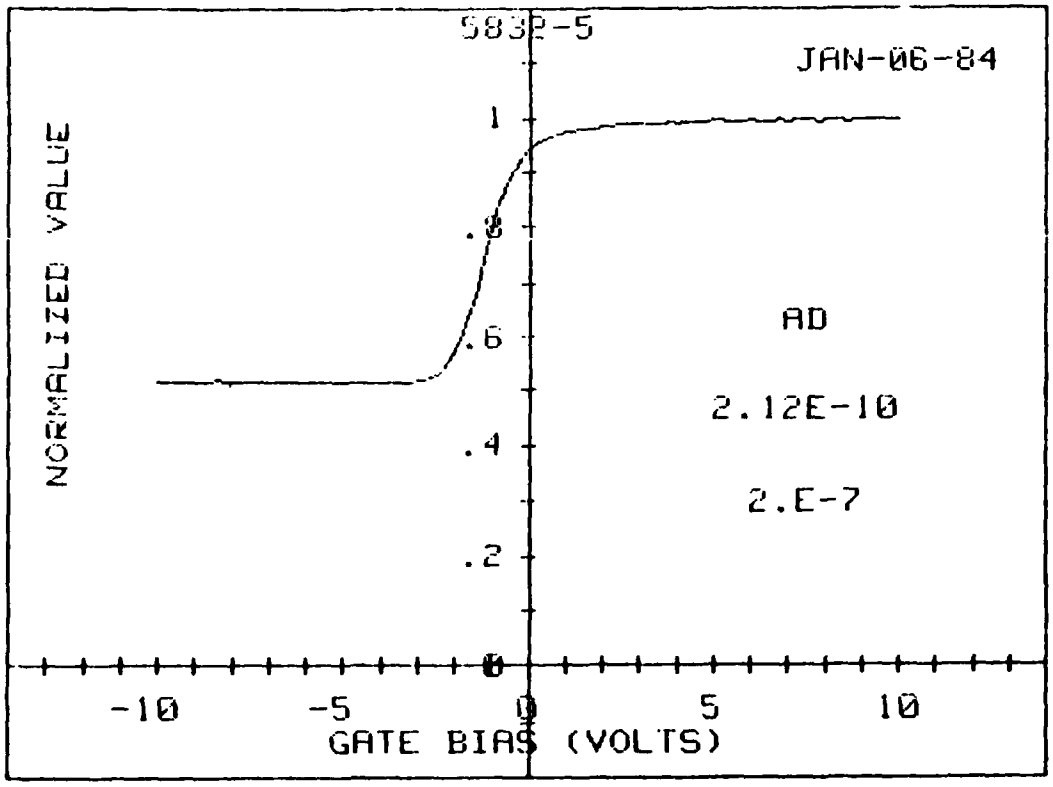


Figure 4.29 A Typical C-V Curve of a MOS Capacitor

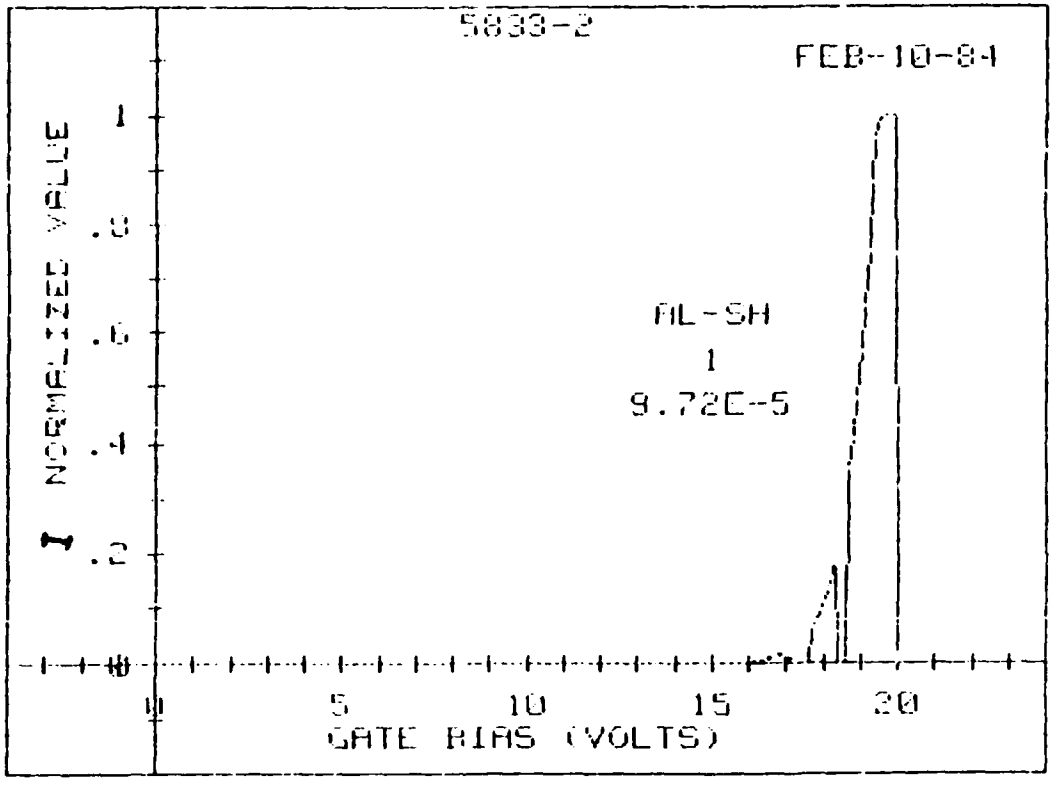


Figure 4.30 A Typical I-V Curve for a MOS Capacitor

few current peaks at the fields just below the intrinsic breakdown field. In most cases, this type of I-V curves was repeatable many times reversibly if the current was limited to $<10^{-4}$ amperes. Once the current increased beyond 10^{-4} amperes, usually the breakdown occurred irreversibly and the MOS capacitor was completely shorted without any self-healing sign. This type of measurements will provide valuable information on intrinsic dielectric breakdown mechanisms and charge injection/trapping for $Si-SiO_2$ systems.

4.5 MEASUREMENTS ON MOSFETs

The DC I-V characteristics were measured for selected MOSFETs and lateral bipolar transistors. Figures 4.31 and 4.32 show typical results.

Two accelerated life tests (at 175°C with $V_{GS} = V_{DS} = -5$ volts, and at 150°C with $V_{GS} = V_{DS} = -5$ volts) on selected samples of p-channel MOSFETs in a packaged chip were performed. The results on failure events were not of any interest because no MOSFET failed during a total test period of more than a week. During this time, the threshold voltage and the subthreshold leakage current of the MOSFETs were periodically measured at 150°C and $V_{GS} = V_{DS} = -5$ volts. Using a HP test system and HP TEACAP software, the drain current was measured and stored in the floppy disk at a fixed drain voltage $V_{DS} = -0.1$ volt and varying gate voltage $V_{GS} = 0$ to -5 volts with 0.2 volt step. Figure 4.33 shows a typical I_D vs. V_{GS} curve from which the threshold voltage of the transistor were determined. From the threshold voltage shift, the oxide charge increase can be calculated. From the sub-threshold voltage swing in the sub-threshold region, the interface state density can be estimated. Each measurement took approximately 10 minutes. During each measurement, the bias voltage was turned-off. Table 4-5 summarizes the result of the recorded threshold voltage values. Since the threshold voltage change is <0.01V as seen from the Table 4-5, the oxide charge density shift ΔQ_{ox} is:

$$\Delta Q_{ox} = C_{ox}\Delta_T < 10^9 \text{ q/cm}^2$$

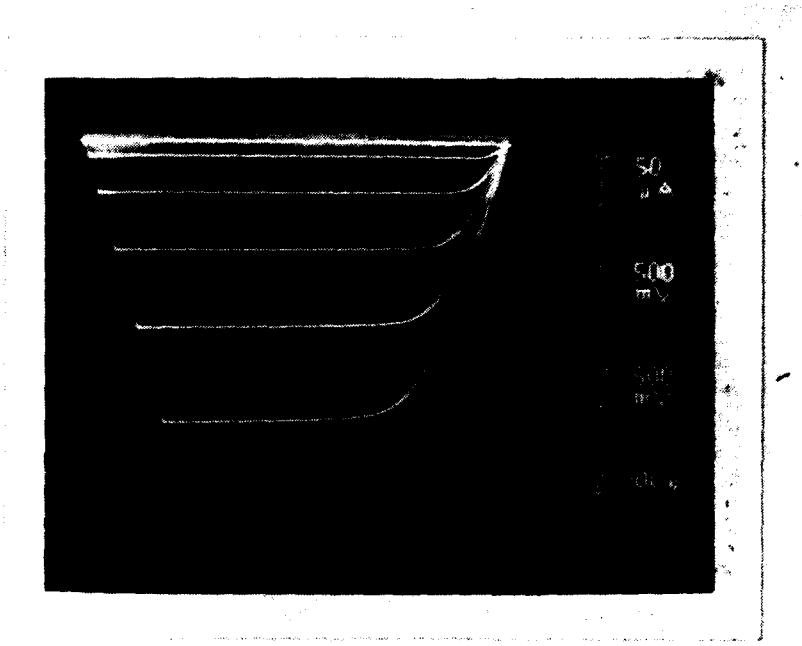


Figure 4.31 A Typical P-Channel MOSFET DC Characteristics

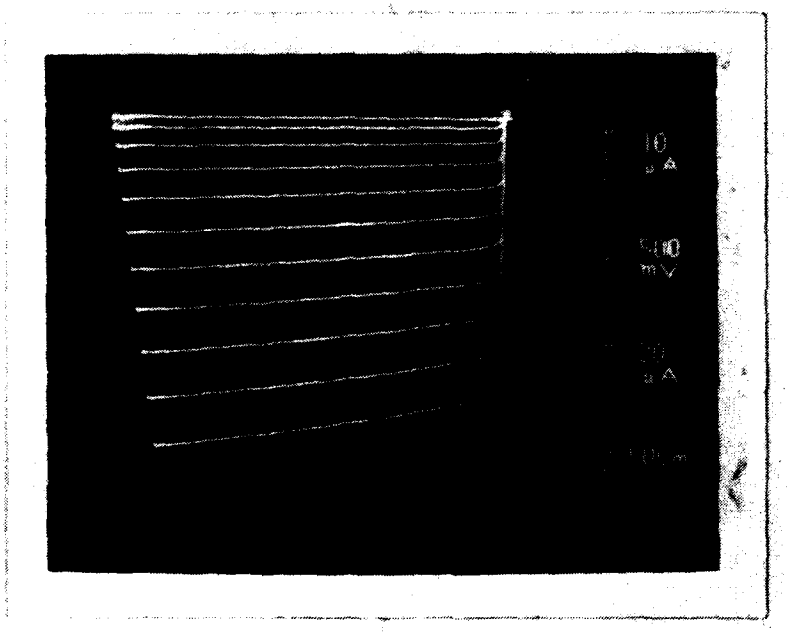


Figure 4.32 A Typical DC Characteristics of a P-N-P Lateral Bipolar Transistor

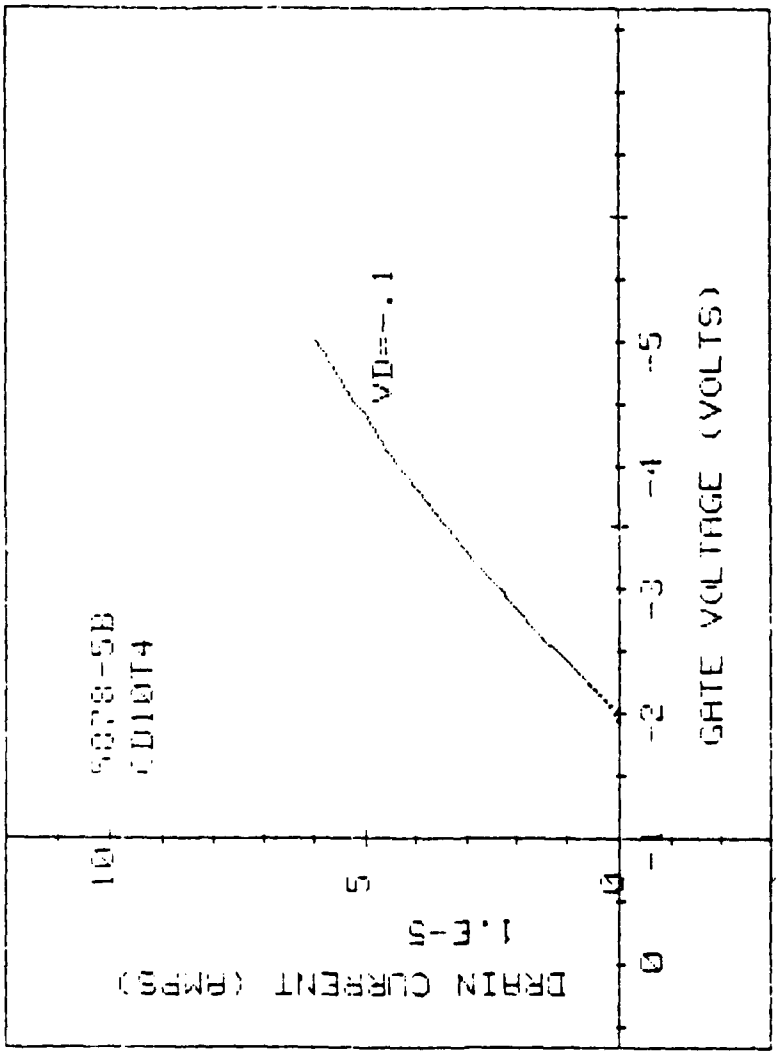


Figure 4.33 A Typical I_D vs V_{GS} Curve

Table 4-5. Temporal Change of Threshold Voltages

$T = 150°C$, $V_D = V_G = -5V$

Time (Min)	Threshold Voltage (Volts)	
	Device A	Device B
0	1.83	1.78
221	1.83	1.78
1160	1.83	1.78
1440	1.83	1.78
1502	1.83	1.78
1760	1.83	1.78
2606	1.83	1.77
2810	1.83	1.77
3080	1.83	1.77

Device A: PMOSFET on Wafer #5878-2
$L = 8\mu m$, $W = 40\mu m$, $X_{ox} \simeq 20.0nm$

Device B: PMOSFET on Wafer #5878-5
$L = 8\mu m$, $W = 40\mu m$, $X_{ox} \simeq 20.0nm$

5.0 DISCUSSION, CONCLUSIONS, AND RECOMMENDATIONS

5.1 DISCUSSION

One of the key accomplishments in this program is the detection of a definitive correlation between the TDDB and the substrate type in the ramp test results. We believe that this finding is the first experimental conclusive evidence of the substrate effects on the TDDB failure of the gate oxide by ramp test, even though the substrate effects have been suggested for some time in the literature and recently by Yamabe et. al [7]. From the ramp data presented in Section 4, we have found that most of the ramp histograms for MOS capacitors, fabricated on the Czochralski substrate and having a gate oxide thickness >30.0nm, show a definitive enhancement of failure in the intermediate field near 7MV/cm, manifesting itself as a bulge in the cumulative fractional failure vs. field histogram, but the capacitors fabricated on the float zone substrate do not show the bulge. Since the electrical field in the ramp histogram is equivalent to the time in the failure vs. time-to-fail plot in the life test according to Berman [1], the bulge indicates an enhanced TDDB failure. The only difference between the two substrate type we have used in this work is that the Czochralski wafers are known to have a higher oxygen impurity content than the float zone wafers. Our oxygen analysis has shown that indeed this is the case; approximately 40ppm of oxygen impurities for the Czochralski wafers, <1ppm oxygen impurities for the float zone wafers, and <1ppm of carbon, which is the limit of detectability in our carbon analysis, for both types of substrates. This suggests that the enhanced TDDB failure of the gate oxide may be due to the oxygen impurities in the starting material. The reason why those capacitors having the gate oxide thickness <30.0nm do not show any enhanced TDDB may be that the oxidation time of <30.0nm oxide is too short for the oxygen impurities in the substrate to diffuse over a distance significant enough to affect the gate oxide integrity. Indeed, a failure minimum at 20.0nm and a failure maximum in the oxide failure vs. thickness curve has been published recently [7], which corroborates our ramp test results.

Even though the influence of the oxygen impurities on TDDB is rather convincing from our results, it is not clear at all what is the correct mechanism associated with the oxygen effect. Many physical processes can be

conjectured to explain the TDDB enhancement by the substrate oxygen impurities. The oxygen-induced stacking faults (OSF) at or near the $Si-SiO_2$ interface can act as a sink for the metallic impurities and the aggregates of the metallic impurities lower the barrier height as mentioned in Section 2, thus reducing the dielectric strength of the gate oxide. Also, OSFs at the interface can increase interface asperity (zig-zag topology) which increases a local field and also changes the interface mechanical stress. The impurity diffusion into the bulk of the gate oxide has also been suggested to be responsible for the degradation of the gate oxide [6,7]. At the present, because of very limited data, it is not possible to say much about the physical mechanisms involved. For this, further extensive data on TDDB are required.

Even though the accelerated life test results are limited, the following is an attempt to predict the use life of our MOS devices by using the accelerated life test data shown in Section 4 as an exercise. From our data at T = 175°C and E = 5MV/cm for MOS capacitors having a gate area of $1x10^{-3}cm^2$, the time-fo-fail for a 40% failure is approximately 10 minutes. If we assume that Q = 0.3ev and A_F = 4decade/MV/cm, the 40% fail use life of the devices having a gate area of $1x10^{-3}cm^2$ at the use condition of T = 25°C and E = 2MV/cm will be from Eq (2-3)

$$t(40\%) = 10x\exp[0.3/k(1/278-1/448)]x10^{12}min \sim 10^{15}min \sim 10^{9} \text{ years!!}$$

For use field E = 3MV/cm, $t(40\%) \sim 10^5$ years; for E = 4MV/cm, t(40%) ~10 years. This calculation shows just how sensitive the predicted life is to the field acceleration factor and the use field. Therefore, unless the correct value for the acceleration factor is available, the projection of the MOS device reliability based on the field-biased accelerated life test is unreliable. Furthermore, the expression in Eq. (2-1) and Eq. (2-3) may not be correct, for the separation of variables in T and E is not justified at all from the physics viewpoint. Indeed, the γ factor in Eq. (2-5) has been reported to be temperature-dependent [1,3].

5.2 CONCLUSIONS

By a series of ramp tests, it was established that a correlation exists between the TDDB and the oxygen contents of the starting materials. However, the physical mechanisms involved in the TDDB are not clear at all. Unless the correct mechanisms are clarified and understood, the dielectric reliability prediction of gate oxides in complex MOS VLSI circuits are not of much practical use. We believe that the physics of TDDB phenomenon in SiO_2 has not been well understood to date. Therefore, any future effort should be directed at determining the correct mechanism or mechanisms of failure.

5.3 RECOMMENDATIONS

Further studies in the following areas are recommended:

- Substrate effects data for a wider range of oxygen content, 1ppm to 100ppm.
- Substrate effect for O_2/HCl grown gate oxide.
- Substrate effect for gate oxide thickness range 10.0nm-50.0nm.
- The effect of mechanical stress on TDDB.
- The effect of interface states and oxide charge on TDDB.

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